- Wide Supply Voltage Range: 4.5V - 24V
- 4A Peak Source Current and 4A Peak Sink Current
- Dual Input Configuration: Non-Inverting (IN+) or Inverting (IN-) Input
- Negative Input Voltage Capability: Down to -5V
- TTL Input-Logic Threshold
- Propagation Delay: 12ns
- Fast Rising and Falling Time: 9ns and 6ns
- Low Quiescent Current: 38uA
- Under Voltage Lock Out Protection of Supply Voltage
- Output Low When Input Floating
- Thermal Shutdown Protection: 170°C
- Available in TSOT23-5L Package

- Power MOSFET Gate Driver
- IGBT Gate Driver
- GaN Device Gate Driver
- Switching Power Supply
- Motor Control, Solar Power

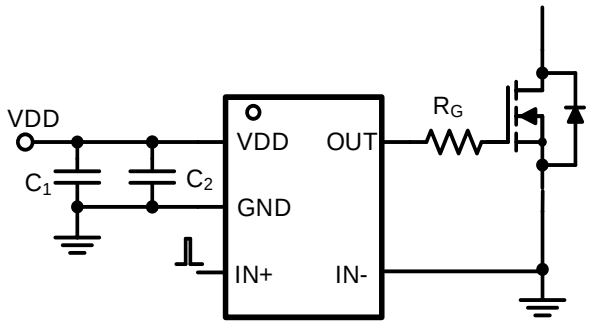
The SCT51240 is a wide supply, single channel, high speed, low side gate driver for power MOSFET, IGBT, and wide band-gap device such as GaN. The 24V power supply rail enhances the driver output ringing endurance during the power device transition. The capability to switch below 5V power supply makes the SCT51240 work well for the low voltage threshold power device.

The SCT51240 can source and sink 4A peak current along with rail-to-rail output driving capability. The minimum 12ns input to output propagation delay enables it suitable for high frequency power converter application. The SCT51240 features wide input hysteresis that is compatible for TTL low voltage logic. The SCT51240 has the capability to handle negative input down to -5V, which enhances the input noise immunity. The IN+ and IN- input provides the flexibility to configure the SCT51240 either as non-inverting or inverting driver.

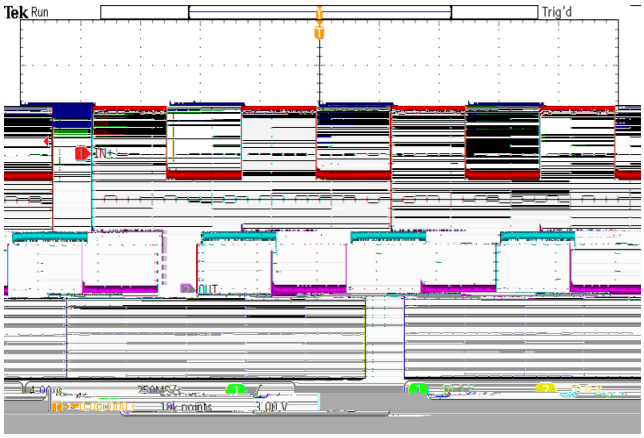
The SCT51240 has very low quiescent current that reduces the stand by power loss in the power converter. The SCT51240 gate driver adopts non-overlap driver design to avoid the shoot-through of output stage.

The SCT51240 features 170°C thermal shut down protection and operates over a wide temperature range -40°C to 150°C. The SCT51240 is available in TSOT23-5L package.

SCT51240 Typical Application



Application Waveform



NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0 Released to Production.
Revision 1.3: Page 8 Table 1, Page 9 input stage description
Revision 1.4: Add high limit for I_Q and RO in EC table

PART NUMBER

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	4.5	24	V
$V_{IN+,IN-}$	Input voltage range	-5	24	V
T_J	Operating junction temperature	-40	150	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)	-1	+1	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

PARAMETER	THERMAL METRIC	TSOT23-5	UNIT
R	Junction to ambient thermal resistance (1)	89	°C/W
R	Junction to case thermal resistance (1)	39	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT51240 is mounted, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT51240. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

V_{DD}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{DD}	Operating supply voltage		4.5		24	V
V_{DD_UVLO}	Input UVLO Hysteresis	V_{DD} rising		4.2 300	4.5	V mV
I_Q	Quiescent current	IN+=IN-=GND or IN+=IN-=VDD, VDD=3.5V, T_J=25°C		38	50	uA
		IN+=IN-=GND or IN+=IN-=VDD, VDD=3.5V, T_J=-40°C~125°C		38	65	uA
		IN+=IN-=GND, V_{DD}=12V		120	190	uA
INPUTS						
V_{IN+}						

V_{DD}=12V, T_A= 25°C.

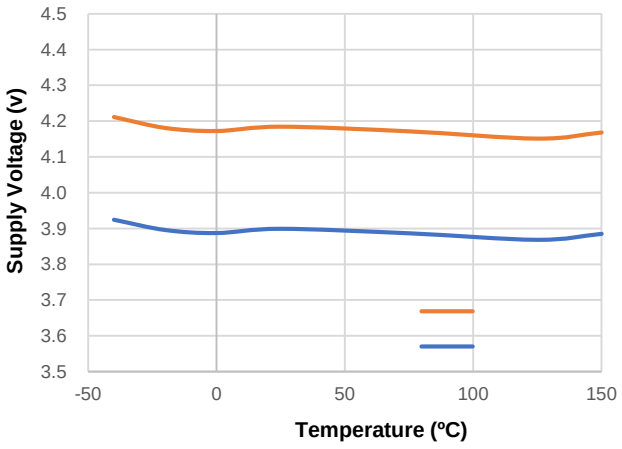


Figure 1. UVLO Vs Temperature

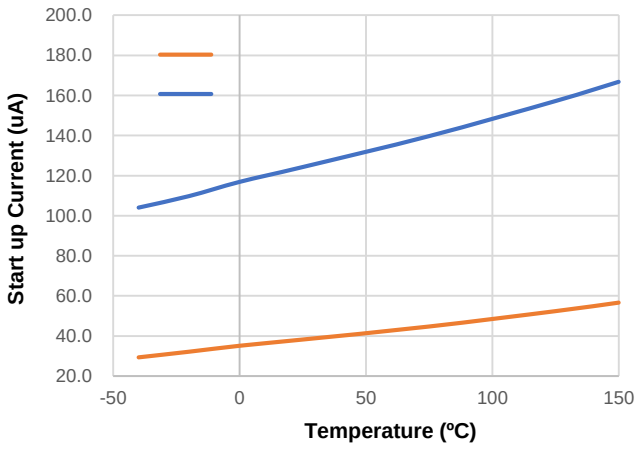


Figure 2. Start-up current Vs Temperature

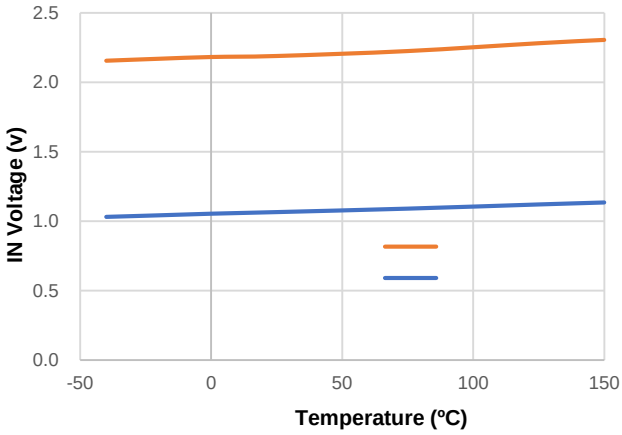


Figure 3. IN Threshold Vs Temperature

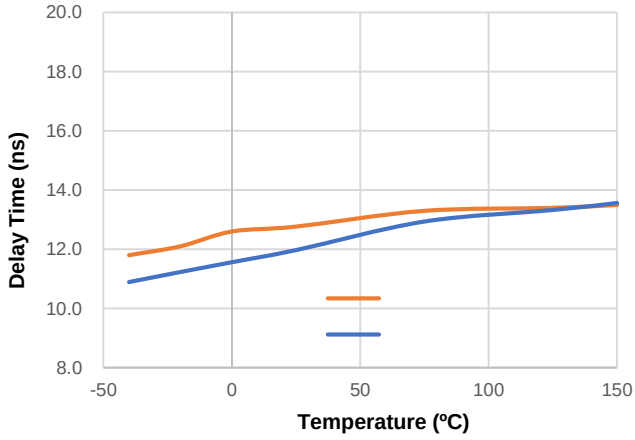


Figure 4. Input to Output Propagation Delay vs Temperature

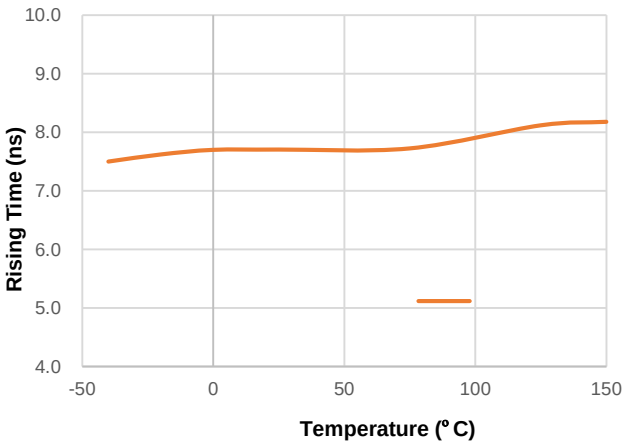


Figure 5. Output Rising Time Vs Temperature

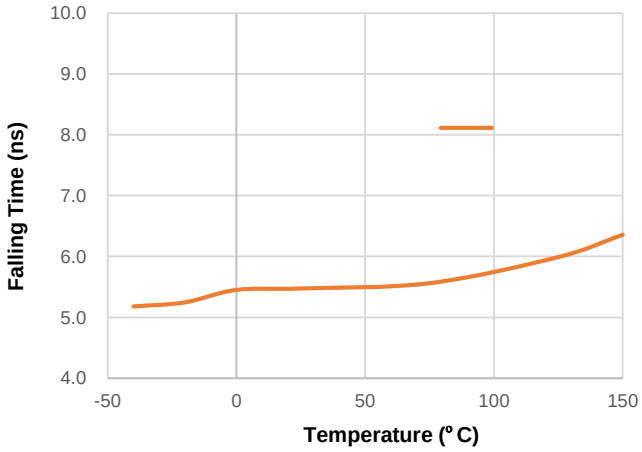
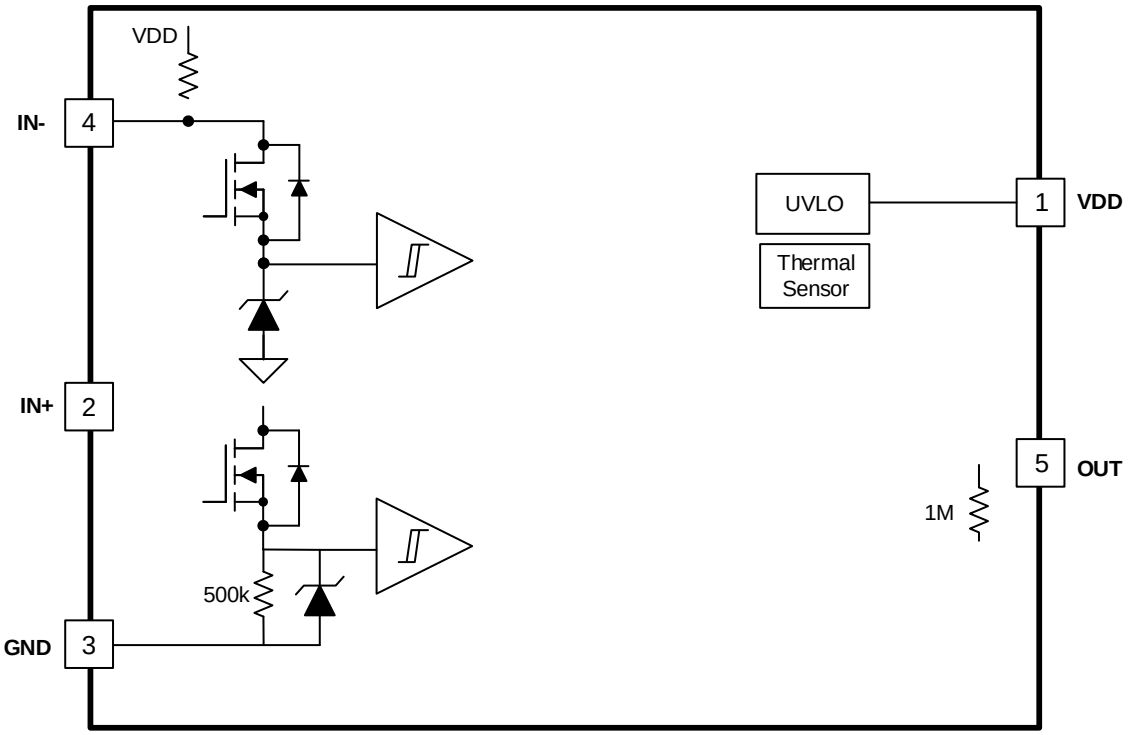


Figure 6. Output Falling Time Vs Temperature

Figure 7. ROH



Overview

The SCT51240 is a up to 24V wide supply, single channel, high speed, low side gate driver for power MOSFET and IGBT. The SCT51240 can source and sink 4A peak current along with the minimum propagation delay 12ns from input to output. The ability to handle -5V DC input increases

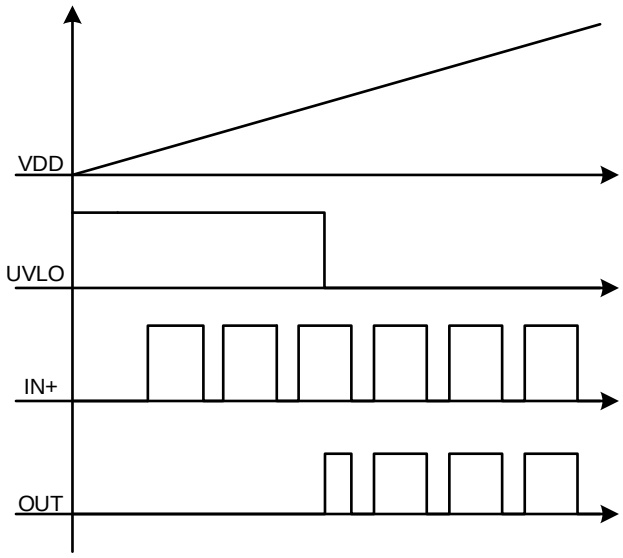


Figure 9. SCT51240 Output Vs VDD

Input Stage

The input of SCT51240 is compatible on TTL logic that is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1.0 V, the logic level thresholds are conveniently driven by PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Input hysteresis provides high noise immunity compared to traditional TTL logic implementation, where the hysteresis is typically less than 0.5 V. SCT51240 also features tight control of the input threshold voltage that ensures stable operation across temperature. The low input capacitance on the input pins increases switching speed and reduces the propagation delay.

The SCT51240 features a dual-input configuration with two input pins available to control the state of the output. The user has the flexibility to configure the device by using either a non-inverting input pin (IN+) or an inverting input pin (IN). The state of the output pin depends on the n the n ab34(n)-32(th)-8ETQotut ic ut091i+q0.-9(iQq(n)Ii)7(c912 0 612 7

(2)

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

If R_G applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

(3)

Where

- R_{OH} is the equivalent pull up resistance of SCT51240
- R_{OL} is the pull down resistance of SCT51240
- R_G is the gate resistance between driver output and gate of power device.

Application Waveforms

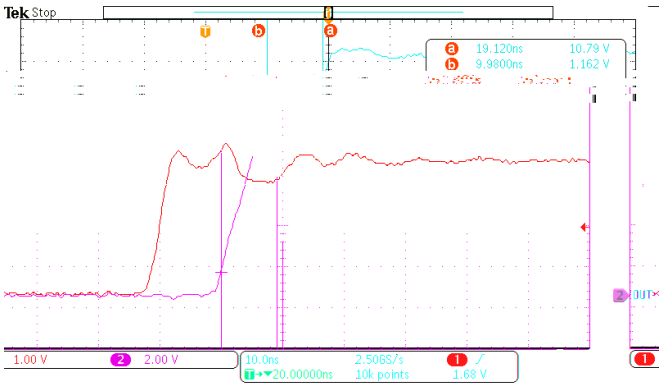


Figure 12. IN+ Switching ON

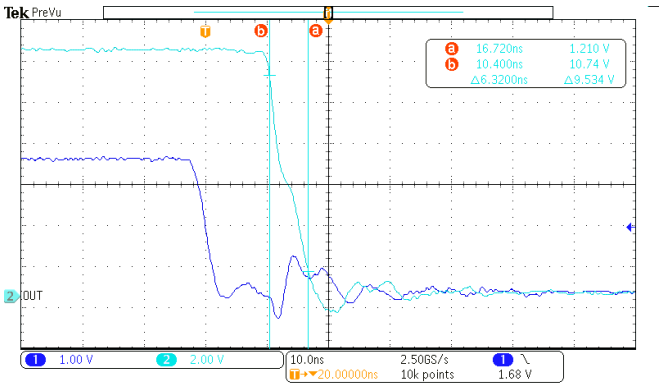


Figure 13. IN+ Switching OFF

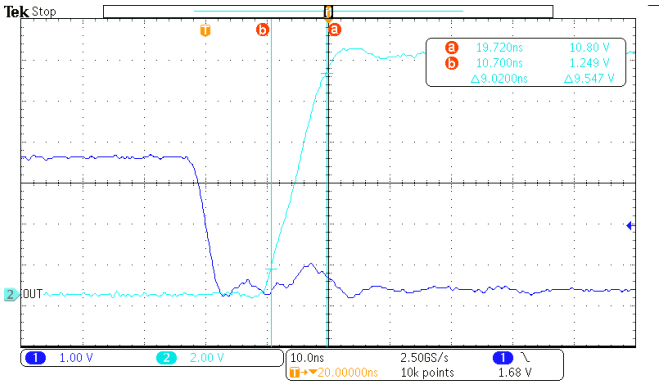


Figure 14. IN- Switching ON

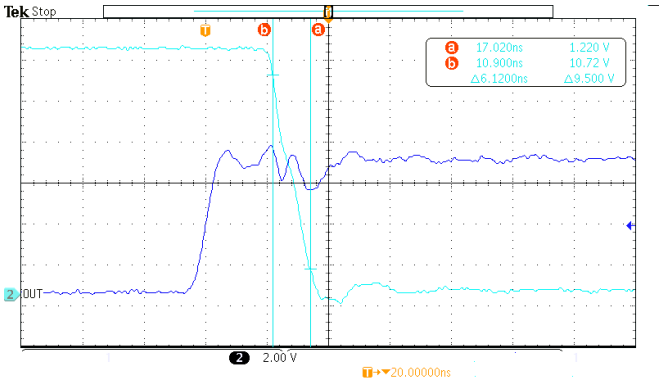


Figure 15. IN- Switching OFF

Layout Guideline

The SCT51240 provides the 4A output driving current and features very short rising and falling time at the power devices gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not optimized. The regulator could suffer from malfunction and EMI noise if the power device gate has serious ringing. Below are the layout recommendations with using SCT51240 and Figure 16 is the layout example.

Put the SCT51240 as close as possible to the power device and minimize the gate driving loop including the driver output and power device gate. The power supply decoupling capacitors needs to be close to the VDD pin and GND pin to reduce the supply ripple.

Star-point grounding is recommended to minimize noise coupling from one current loop to the other. The GND of the driver connects to the other circuit node such as source of power MOSFET or ground of PWM controller at single point. The connected paths must be as short as possible to reduce parasitic inductance. A ground plane provides noise shielding and thermal dissipation as well.

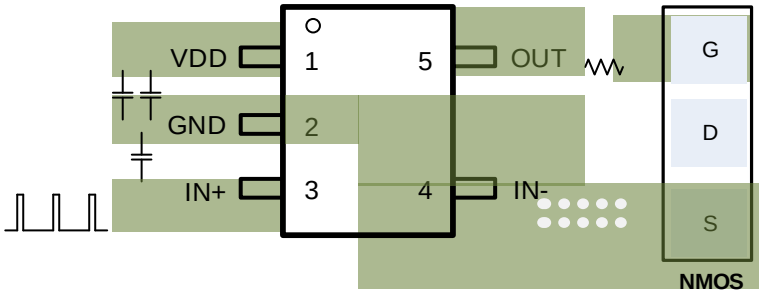


Figure 16. SCT51240 PCB Layout Example

Thermal Considerations

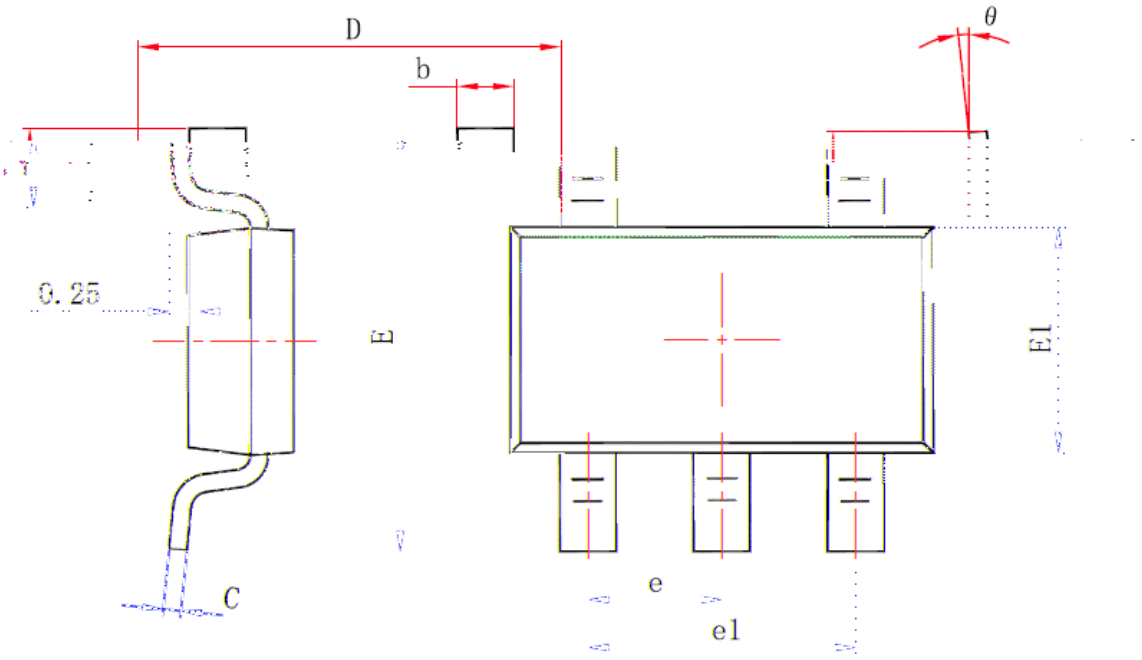
The maximum IC junction temperature should be restricted to 170°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (4).

(4)

where

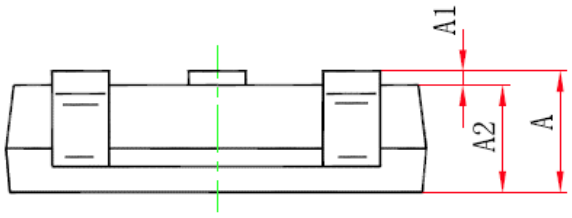
- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, and environmental factor. Soldering the ground pin to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.



TOP VIEW

BOTTOM VIEW

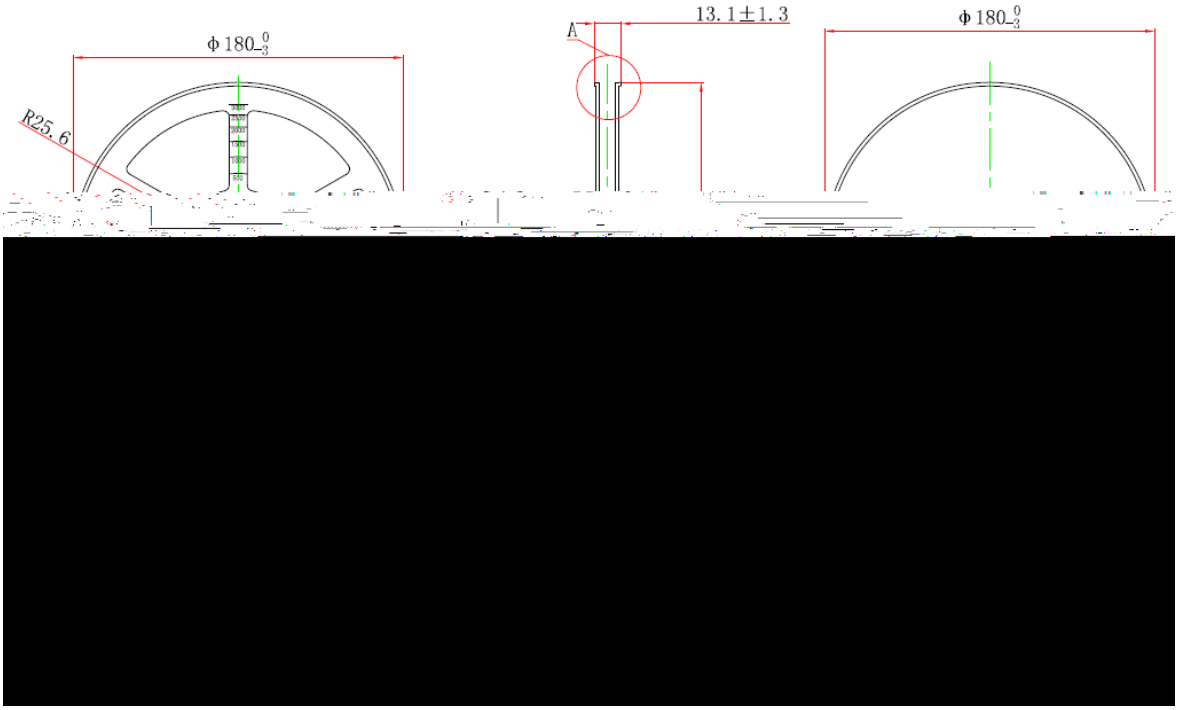


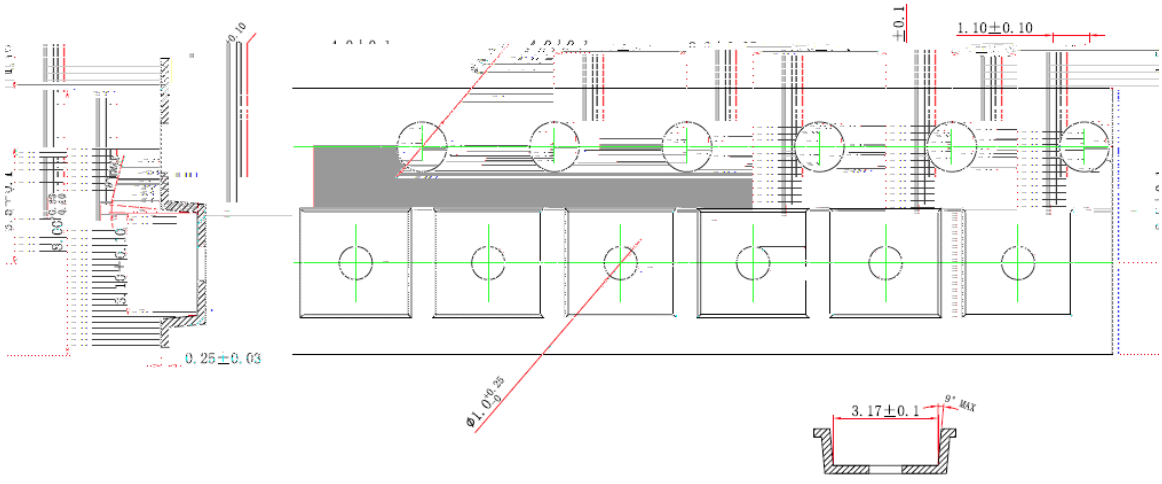
SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	---	---	0.9
A1	0.02	---	0.09
A2	0.7	---	0.8
b	0.35	---	0.5
c	0.08	---	0.2
D	2.82		3.02
E	2.65		2.95
E1	1.6		1.7
e	0.95 (BSC)		
e1	1.90 (BSC)		
L	0.3		0.6
	0°		8°

NOTE:

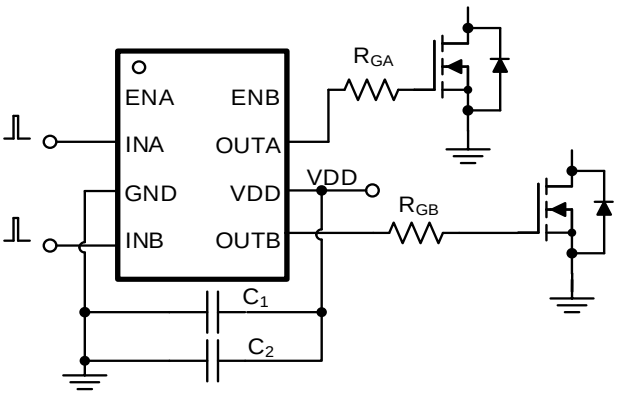
1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

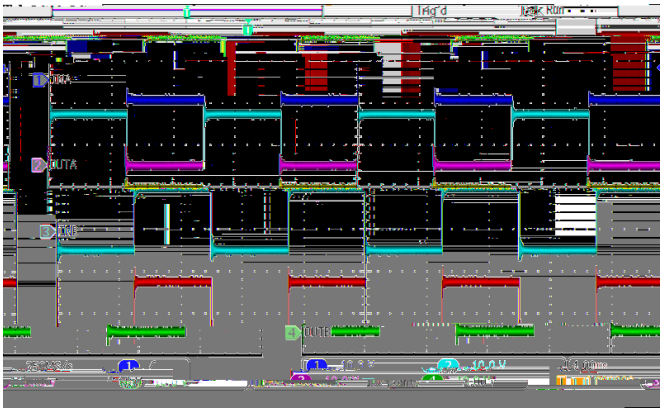




Feeding Direction

SCT52240 Typical Application





PART NUMBERS	DESCRIPTION	COMMENTS
SCT52240	Up to 24V Supply, 4-A Dual Channel High Speed Low Side Driver	• Stackable Output Application • -5V Input Capability