Wide Vin 50V Non-synchronous Boost/Flyback/SEPIC Controller

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide Input Voltage Range: 3.2V-50V
- Low Shutdown Current 3.7uA
- Low Quiescent operating Current: 450uA
-

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 1.0: Released to Market

Revision 1.1: Correct max operating input voltage

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT81620QMTD	1620Q	8-Lead 3mm×3mm Plastic MSOP

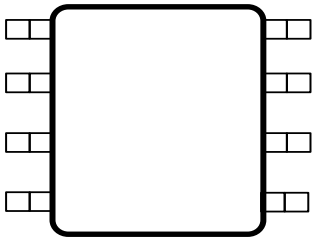
1) For Tape & Reel, Add Suffix R (e.g. SCT81620QMTDR)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	62	V
DR	-1	6.6	V
ISEN, COMP, FB, FA/SYNC/SD	-5	5.5	V
Peak Driver Output Current		1(2)	A
Junction temperature(2)	-40	150	C
Storage temperature T_{STG}	-65	150	C

PIN CONFIGURATION



Top View: 8-Lead Plastic MSOP 3mmx3mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) Guaranteed by design, not tested in productions.
(3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetaxiatier1 -1.174.3 0 TC /P <</MCID 60 >>BDC75-0.002 Tc.15 Td [((8j EMC /P <</MCID 60 >>BDCre TT5 1 Tf 34)Tj 1. 57.1 -57759.2

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.2	50	V
V_{CC}	VCC voltage range	3.2	6.1	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	MSOP-8	UNIT
R	Junction to ambient thermal resistance(1)	132.8	°C/W
R (top)	Junction to case (top) thermal resistance(1)	64.1	°C/W
R B	Junction to board thermal resistance(1)	83.8	°C/W

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT81620Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT81620Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.92		50	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.9 160		V mV
I_{SD}	Shutdown current	$V_{FA/SYCN/SD}$=5V		3.7	8	uA
I_Q	Quiescent current from VIN	no load, no switching		460		uA
Reference and Control Loop						
V_{REF}	Reference voltage of FB	Tj=25°C	1.241	1.26	1.278	V
		Tj=-40~125°C	1.222		1.297	
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{ON_MIN}	Minimum on-time	Fsw=400kHz		250		ns
Protection						
V_{OVTH}(3)	FB overvoltage threshold	FB rising	25	85	135	mV
		Hysteresis	30	80	130	mV
T_{SD}(1)	Thermal shutdown threshold	T_J rising		165		°C
	Hysteresis			25		°C

(1) Guaranteed by design and bench, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) The overvoltage protection is specified with respect to the feedback voltage. This is because the overvoltage protection tracks the feedback voltage. The overvoltage threshold can be calculated by adding the feedback voltage (V_{FB}) to the overvoltage protection specification.

TYPICAL CHARACTERISTICS

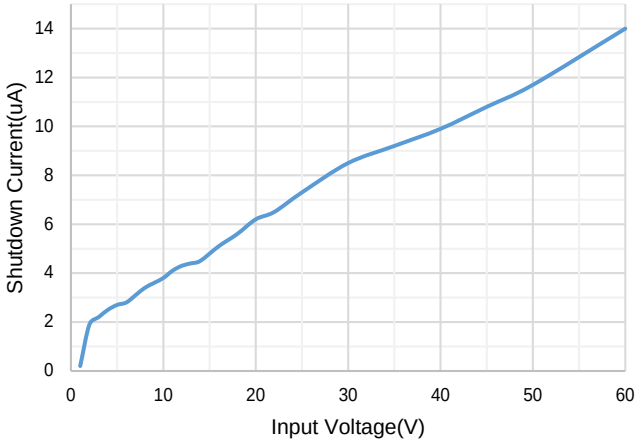


Figure 1. ISD vs Input Voltage

Figure 2. IQ vs Input Voltage

Figure 3. Switching Frequency vs RT

Figure 4. Switching Frequency vs Temperature

Figure 5. Efficiency vs Load Current, Boost, VOUT=12V

Figure 6. Efficiency vs Load Current, Sepic, VOUT=12V

TYPICAL CHARACTERISTICS

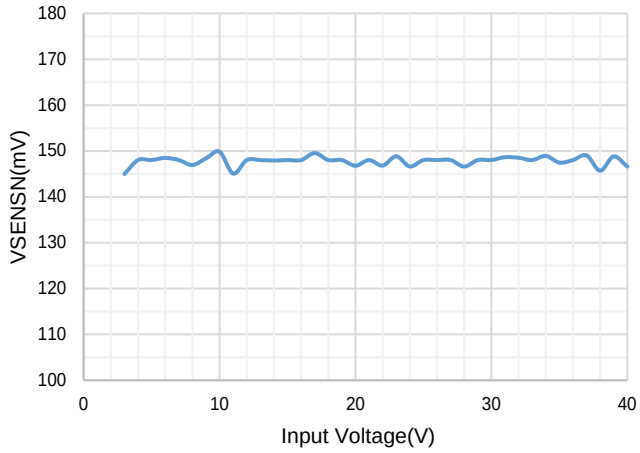


Figure 7. VSENSN vs Input Voltage

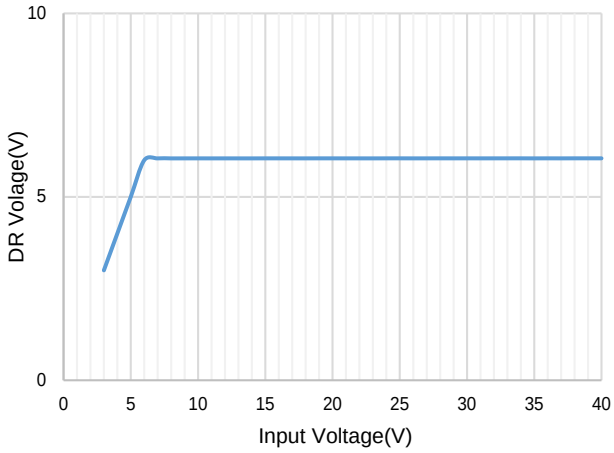


Figure 8. DR Volage vs Input Voltage

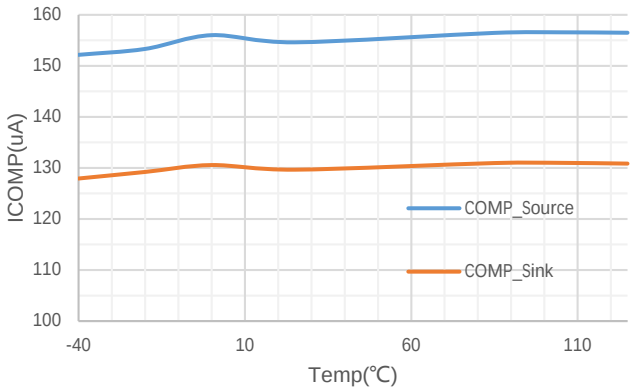


Figure 9. COMP Current vs Temperature

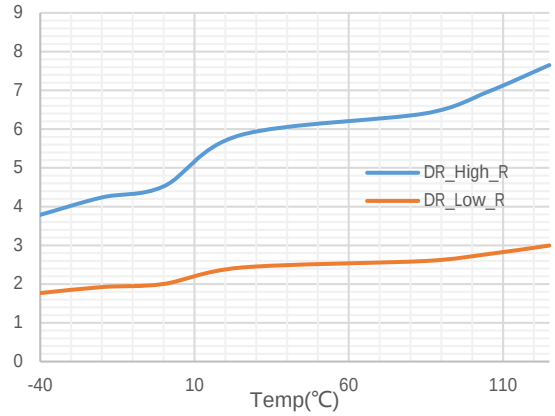
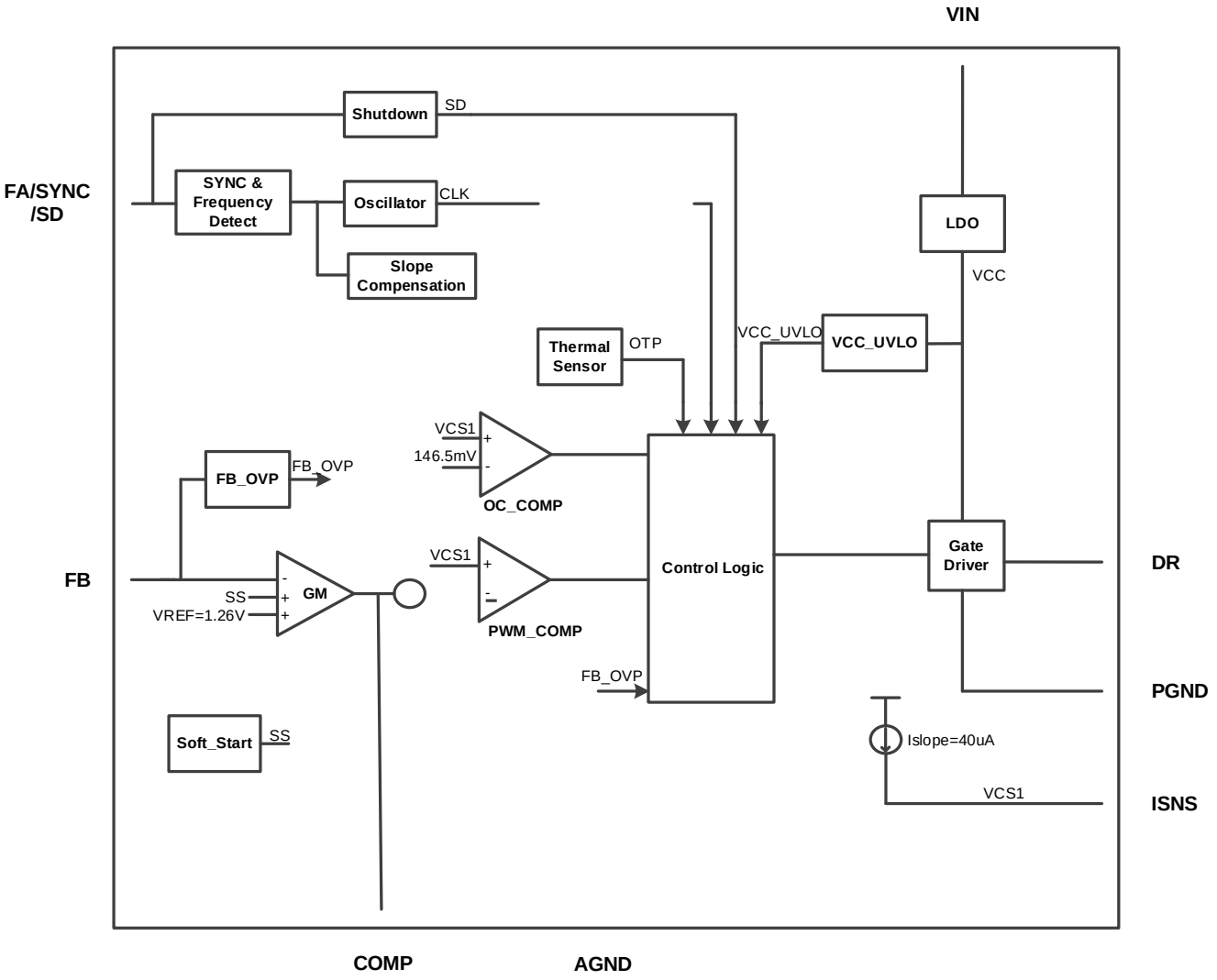


Figure 10. DR Resistance vs Temperature

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Overview

The SCT81620Q device is a wide input range, non-synchronous boost controller that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies.

In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the ISNS pin. This voltage is fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input. The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch using the switch logic block. This forces a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off. The voltage sensed across the sense resistor generally contains spurious noise spikes, these spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration is called the blanking interval and is specified as minimum on-time in the Electrical Characteristics section. Under extremely light-load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET in on during the blanking interval is more than what is delivered to the load. An over-voltage comparator inside the SCT81620Q prevents the output voltage from rising under these conditions. The over-voltage comparator senses the feedback (FB pin) voltage and resets the RS latch. The latch remains in reset state until the output decays to the nominal value.

The SCT81620Q works at Pulse skip mode to further increase the efficiency in light load condition. The quiescent current of SCT81620Q is 450uA typical under no-load condition and not switching. Disabling the device, the typical supply shutdown current on VIN pin is 3.7 A.

Overvoltage Protection

The SCT81620Q has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (FB). If at any time the voltage at the feedback pin rises to 1.345V (typ.), OVP is triggered. OVP will cause the DR pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The SCT81620Q begins switching again when the feedback voltage reaches 1.265V (typ.).

Slope Compensation Ramp

The SCT81620Q uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. However, current mode control has a Sub-harmonic Oscillation when duty cycles greater than 50%. To prevent the Sub-harmonic oscillations, a compensation ramp is added to the control signal.

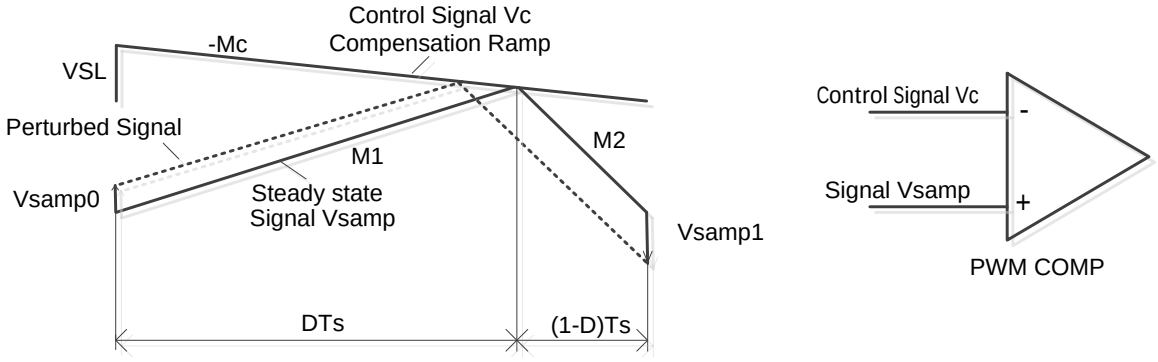


Figure12. Sub-Harmonic Oscillation for D>0.5 and Compensation Ramp to Avoid Sub-Harmonic Oscillation

The current mode control scheme samples the inductor current, IL, and compares the sampled signal, Vsamp, to a internally generated control signal, Vc. The current sense resistor, RSEN, as shown in Figure11 converts the sampled inductor current, IL, to the voltage signal, Vsamp, that is proportional to IL such that

$$V_{samp} = I_L * R_{SEN} \quad (1)$$

Figure12 illustrate the theory why Sub-Harmonic Oscillation happen, the rising and falling slopes, M1 and -M2 respectively, of Vsamp are also proportional to the inductor current rising and falling slopes, Mon and -Moff respectively. Where Mon is the inductor slope during the switch on-time and -Moff is the inductor slope during the switch off-time and are related to M1 and -M2 by

$$M_1 = M_{on} * R_{SEN} \quad (2)$$

$$-M_2 = -M_{off} * R_{SEN} \quad (3)$$

For the boost topology:

$$M_1 = M_{on} * R_{SEN} = Vin * R_{SEN} / L \quad (4)$$

$$M_2 = M_{off} * R_{SEN} = (Vout - Vin) * R_{SEN} / L \quad (5)$$

In Figure10, a small increase in the load current causes the sampled signal to increase by Vsamp0. The effect of this load change, Vsamp1, at the end of the first switching cycle is

$$\Delta V_{samp1} = -(\frac{M_2 - M_c}{M_1 + M_c}) * \Delta V_{samp0} \quad (6)$$

So, When No compensation ramp signal is added, which Mc is zero, then:

$$\Delta V_{samp1} = -(\frac{M_2}{M_1}) * \Delta V_{samp0} = -(\frac{D}{1-D}) * \Delta V_{samp0} \quad (7)$$

When D > 0.5 Vsamp1 will be greater than Vsamp0. In other words, the disturbance is divergent. So a very small perturbation in the load will cause the disturbance to increase.

After a compensation ramp is added to the control signal. To ensure that the perturbed signal converges we must maintain:

$$\left| -(\frac{M_2 - M_c}{M_1 + M_c}) \right| < 1 \quad (8)$$

The compensation ramp has been added internally in the SCT81620Q. The slope of this compensation ramp has been selected to satisfy most applications, and it's value depends on the switching frequency. This slope can be calculated using the formula:

$$M_c = V_{SL} * F_s \quad (9)$$

VSL is the amplitude of the internal compensation ramp and FS is the controller's switching frequency.

For more flexibility, slope compensation can be increased by adding one external resistor, RSL, in the ISEN's path.

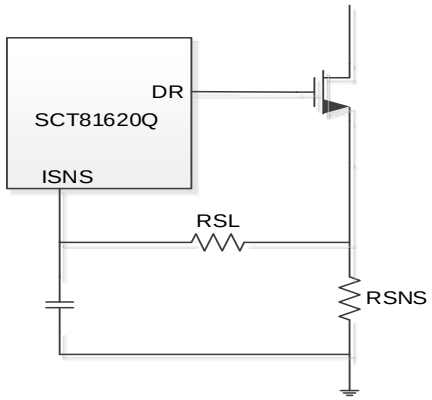


Figure13 .External RSL to increase slope compensation

Adjustable Peak Current Limit

The device provides cycle-by-cycle peak current limit protection that turns off the MOSFET when the sum of the inductor current and the programmable slope compensation ramp reaches the current limit threshold. Peak inductor current limit (IPEAK-CL) in steady state is calculated as shown in:

$$I_{PEAK\_CL} = \frac{V_{SENSE} - 40uA \times R_{SL} \times D}{R_{SNS}} \quad (11)$$

Where

- V_{SENSE} is ISEN pin limiting voltage (Typ.=146.5mV)
- $I_{PEAK-CL}$ is the inductor peak current limit
- R_{SL} is Slope compensation resistor
- D is Duty cycle
- R_{SNS} is the Inductance peak current detection resistance

When overload happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high. When COMP voltage is clamped for 64 cycles, the controller stops working. After remaining OFF for 32768 cycles, the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high after soft start time and COMP still keep high for 64 cycles the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

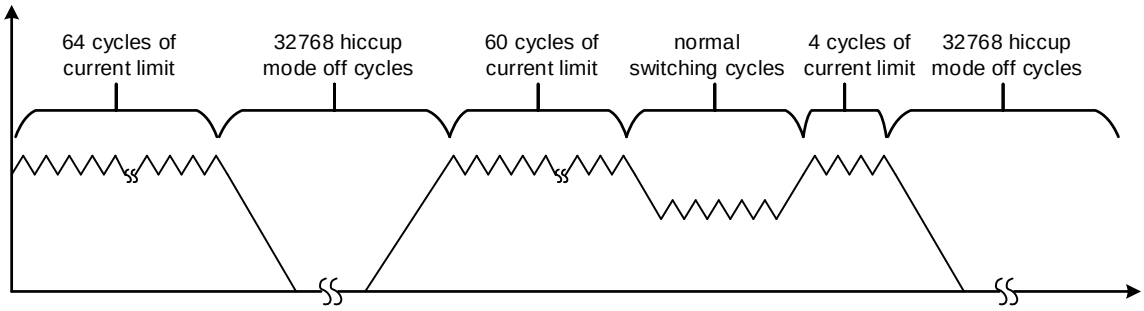


Figure14. Hiccup Mode Protection

Because D can be variable under different Vin, IPEAK-CL is not stable under different Vin when using external slope compensation resistor, so for an accurate peak current limit operation over the input supply voltage, SCT recommends using only the fixed slope compensation.

Output Voltage

The output voltage is set by an external resistor divider RFBT and RFBB in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of RFBT can be calculated by Equation 12.

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (12)$$

where:

- V_{REF} is the feedback reference voltage, typical 1.26V

Frequency Adjust/Shutdown/ Synchronization

The switching frequency of the SCT81620Q can be adjusted between 100 kHz and 2.2 MHz using a single external resistor. This resistor must be connected between the FA/SYNC/SD pin and ground, Equation 13 can be used to estimate the frequency adjust resistor.

$$R_{FA}(k\Omega) = \frac{19700}{fsw(kHz)} - 1.177 \quad (13)$$

The SCT81620Q can also be synchronized to an external clock. The external clock must be connected between the FA/SYNC/SD pin and ground, as shown in Figure 16. The frequency adjust resistor may remain connected while synchronizing a signal, therefore if there is a loss of signal, the switching frequency will be set by the frequency adjust resistor.

The FA/SYNC/SD pin also functions as a shutdown pin. If a high signal (>1.27V) appears on the FA/SYNC/SD pin over 30uS, the SCT81620Q stops switching and goes into a low current mode. The total supply current of the IC reduces to 3.7 µA, typically, under these conditions.

Figure 17 and Figure 18 show an implementation of a shutdown function when operating in frequency adjust mode and synchronization mode, respectively. In frequency adjust mode, connecting the FA/SYNC/SD pin to ground forces the clock to run at a certain frequency. Pulling this pin high shuts down the IC. In frequency adjust or synchronization mode, a high signal for more than 30 µs shuts down the IC.

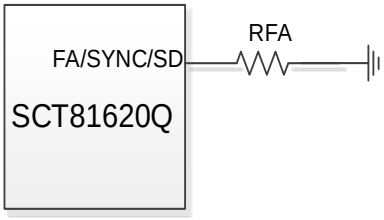


Figure15. Frequency Adjust

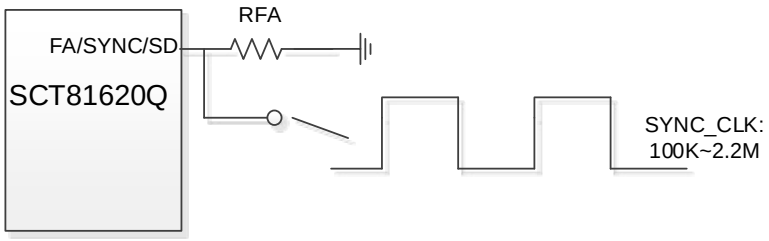


Figure16. Frequency Sync

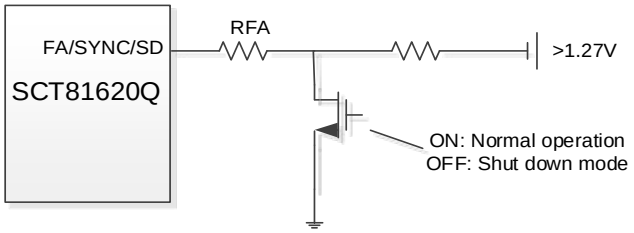
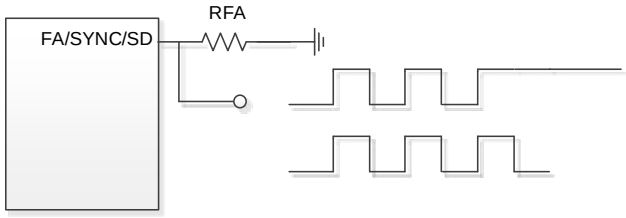


Figure17. Shutdown operation in Frequency Adjust Mode



APPLICATION INFORMATION

Typical Application (Boost)

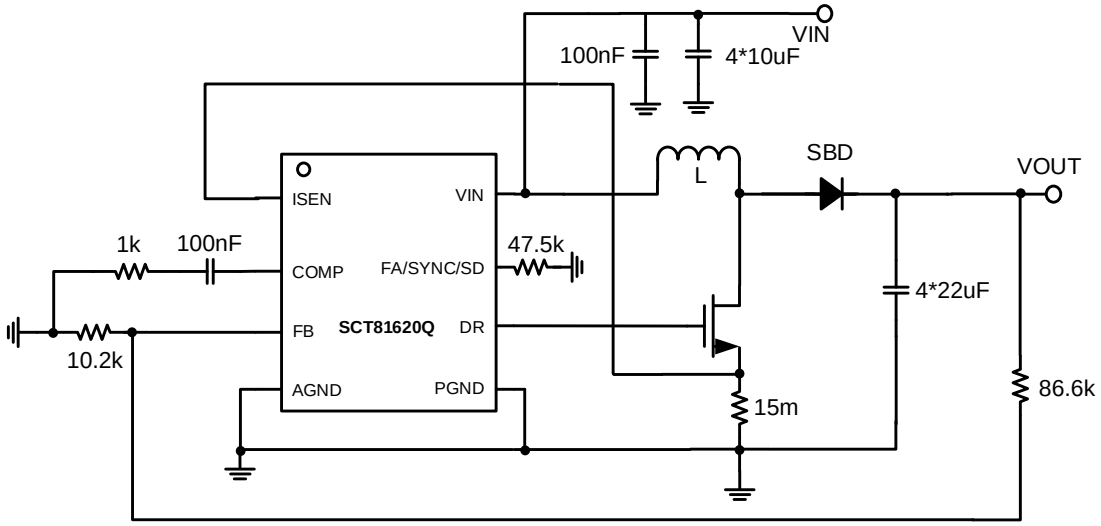


Figure 19. Application Schematic, 3V to 11V, 2A Boost Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 3V to 11V
Output Voltage	12V
Maximum Output Current	3A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

Inductor Selection (Boost)

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

nd-2]TJ (s)62 npu6 116sap6 66 uanu3s

Inductor values can have ±20% or even ±50% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturationatura (i)1.5 (

SCT81620Q

Where

I_G is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current. The peak diode current can be calculated using Equation 24.

$$I_{D(PEAK)} = \frac{I_{OUT}}{(1-D)} + \Delta I_L \quad (24)$$

Thermally the diode must be able to handle the maximum average current delivered to the output. The peak reverse voltage for boost converters is equal to the regulated output voltage. The diode must be capable of handling this voltage. To improve efficiency, a low forward drop schottky diode is recommended.

Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

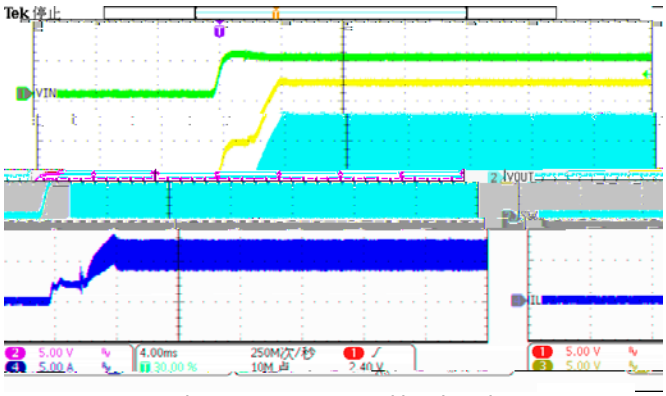


Figure 20. Power up(Iload=2A)

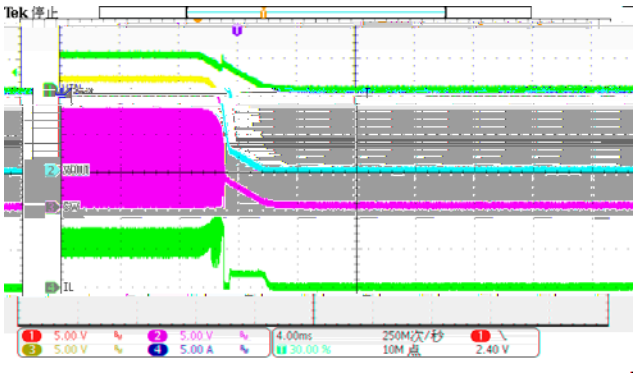


Figure 21. Power down(Iload=2A)

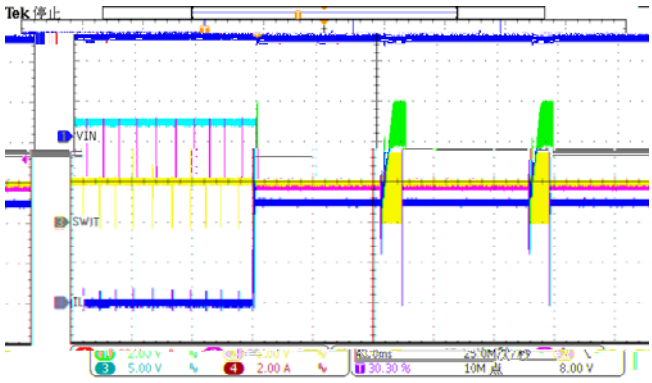


Figure 22. Over current protection (Iload=5A)

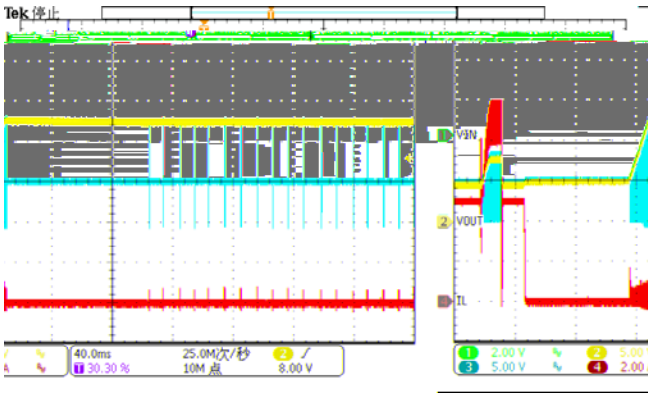


Figure 23. Over current recovery (Iload=5A)

Figure 24. Steady-state (Iload=2A)

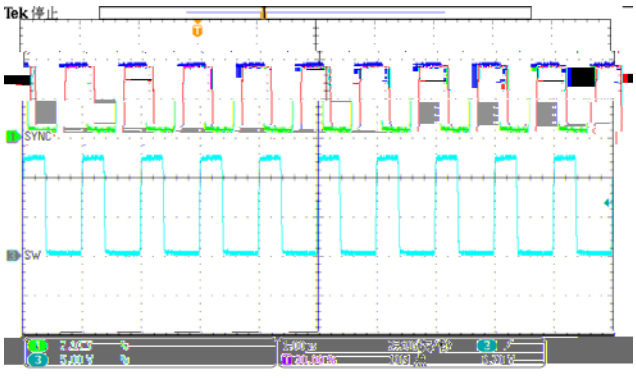


Figure 25. Sync Frequency

Typical Application (Sepic)

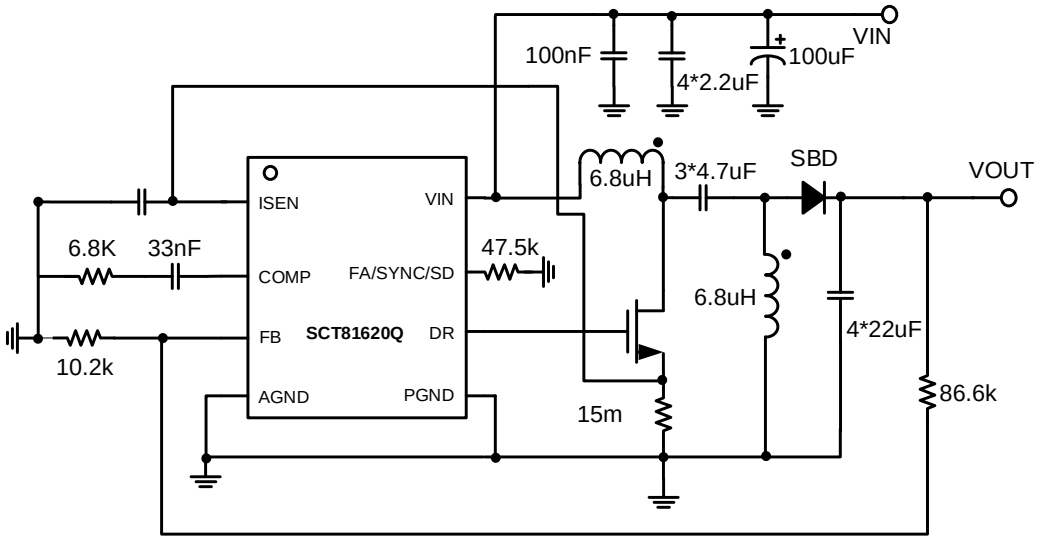


Figure 26. Application Schematic, 5V to 50V, 2A Sepic Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 5V to 50V
Output Voltage	12V
Maximum Output Current	2A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

The diode at the output side must withstand the reverse voltage when the MOSFET is turned-on. The peak reverse voltage is given by:

$$V_{D\_PEAK} = V_{IN\_MAX} + V_{O\_MAX} \quad (35)$$

The diode should also be capable to flow switch peak current IQ_PEAK.

The power dissipation of the diode is equal to the forward voltage drop multiplies output current. Schottky diodes are recommended here to minimize the power loss.

Coupling Capacitor Selection

For ceramic capacitors with low-ESR, the peak to peak voltage ripple on coupling capacitor is estimated by:

$$\Delta V_{CS} = \frac{I_O \times D_{MAX}}{C_S \times f_{SW}} \quad (36)$$

The maximum voltage across the coupling capacitor is maximum input voltage. The voltage rating of the coupling capacitor must be greater than it.

The RMS current of coupling capacitor is given by:

$$\sqrt{\qquad}$$

$$I_{COUT\_RMS} = I_O \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad (41)$$

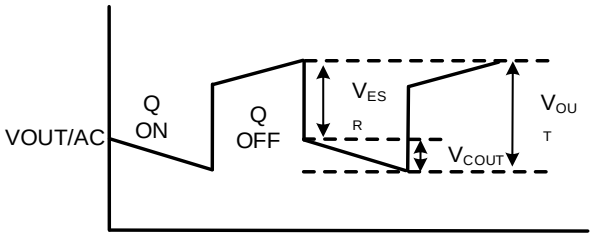


Figure 27. Output Voltage Ripple

Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

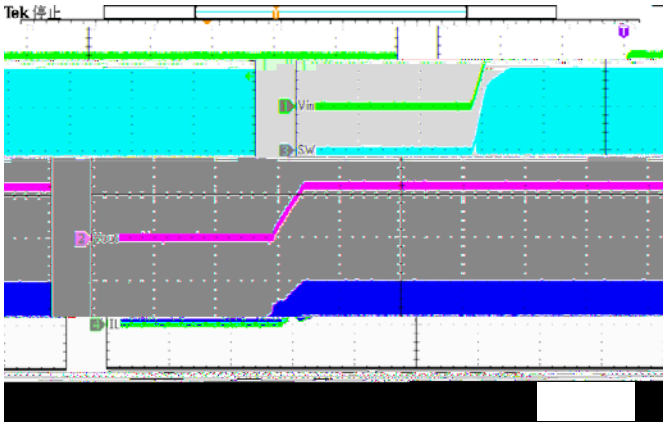


Figure 28. Power up(Iload=2A)

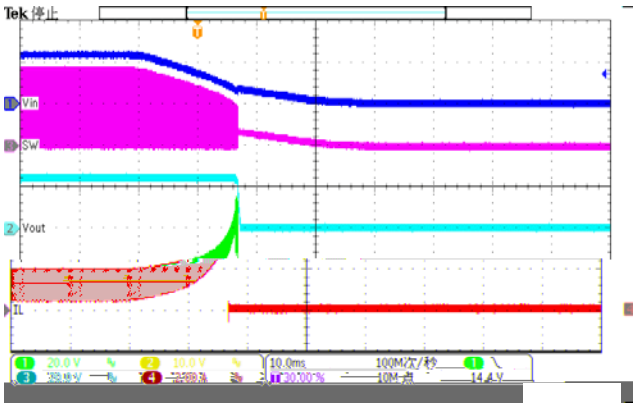


Figure 29. Power down(Iload=2A)

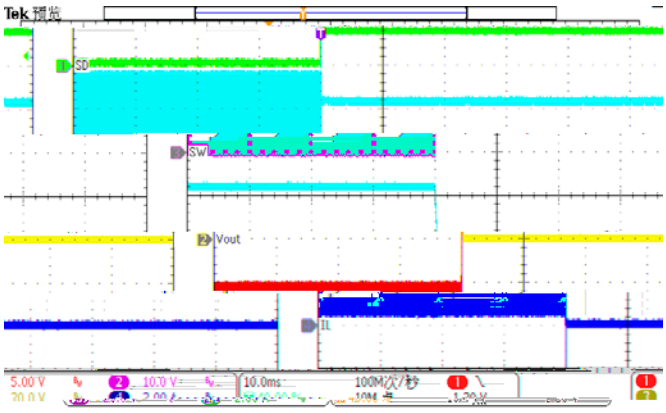


Figure 30. Shutdown remove

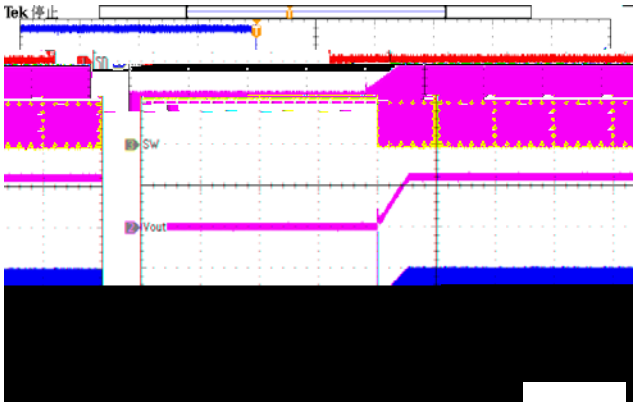


Figure 31. Shutdown remove

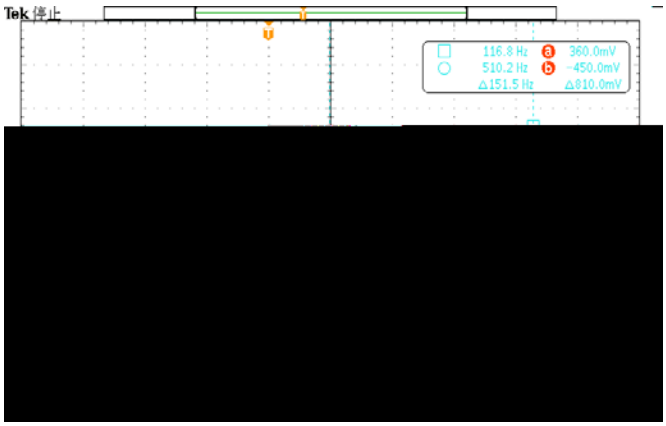


Figure 32. LoadTrans (Iload=0.5A-1.5A)

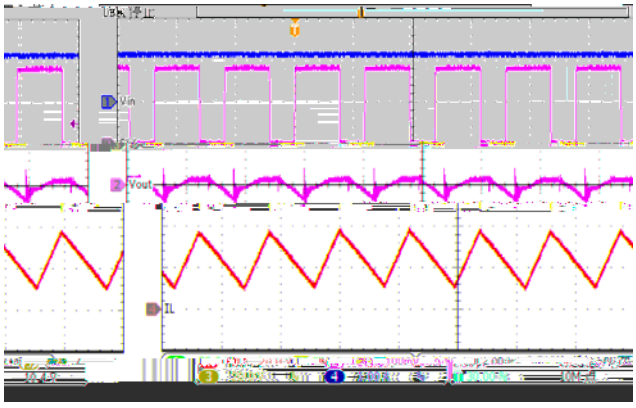
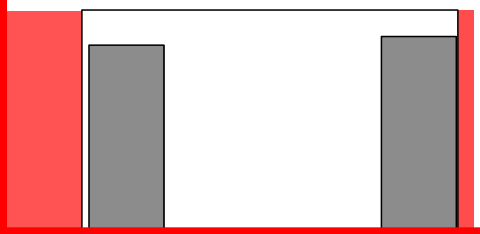
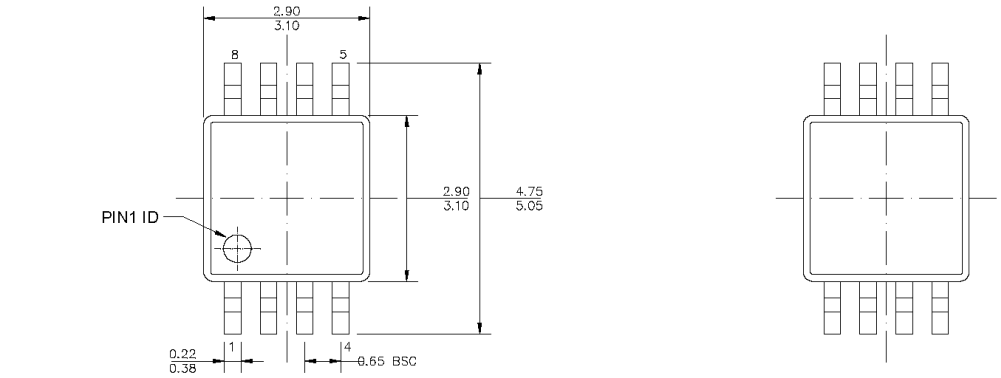


Figure 33. steady-state (Iload=2A)

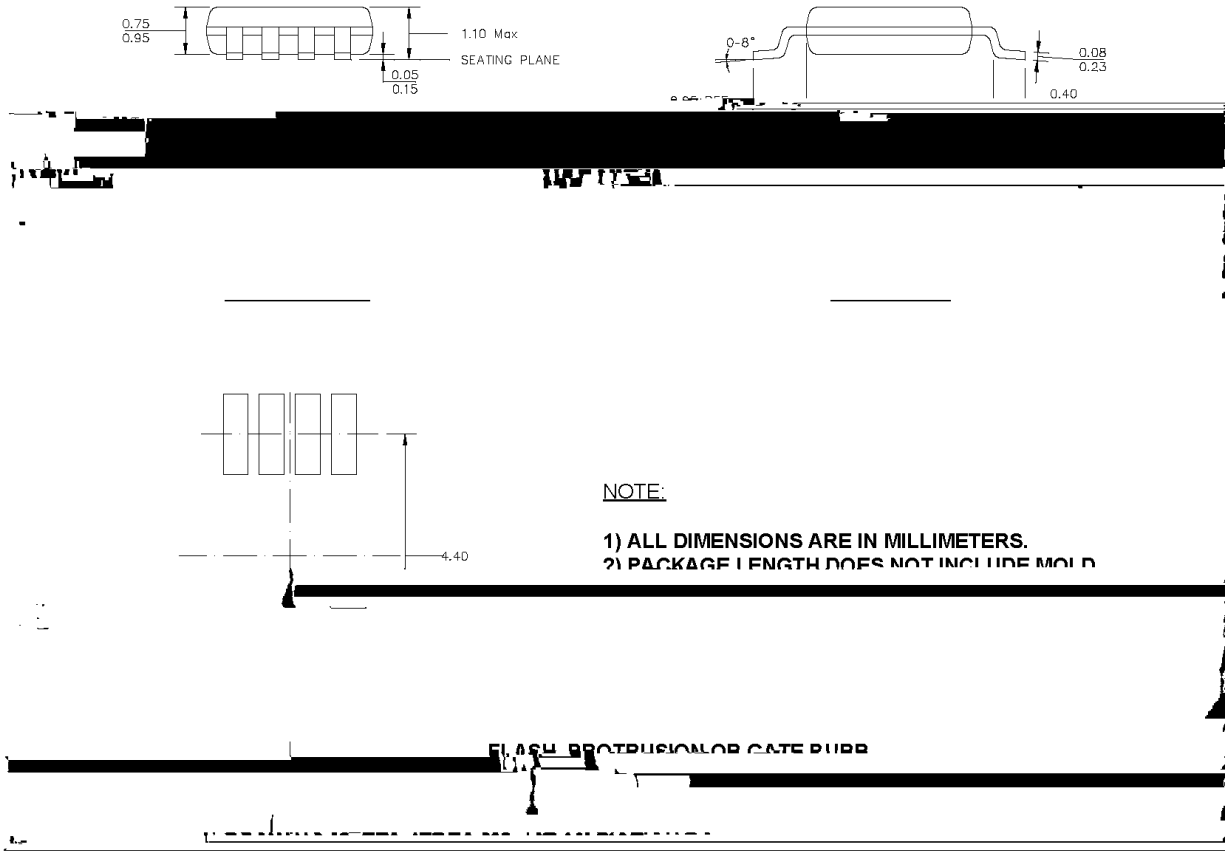


PACKAGE INFORMATION



TOP VIEW

BOTTOM VIEW



TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT81620QMTDR	MSOP	8	4000