5.5V-65V Wide Input Voltage Range Synchronous Buck Controller

FEATURES

REVISION HISTORY

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION

1)

ABSOLUTE MAXIMUM RATINGS

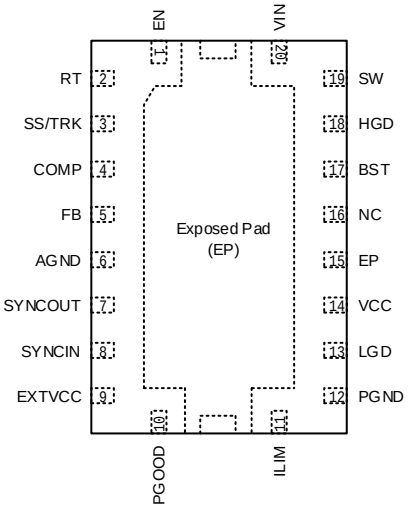
Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	72	V
SW	-1	72	V
SW (20ns transient)	-5	80	V
ILIM	-1	72	V
EN	-0.3	72	V
VCC, EXTVCC,LO	-0.3	14	V
FB, COMP, SS/TRK, RT	-0.3	6	V
SYNCIN	-0.3	14	V
BST	-0.3	86	V
BST to VCC		72	V
BST to SW	-0.3	14	V
VCC to BST (20ns transient)		7	V
LO (20ns transient)	-3		V
PGOOD	-0.3	14	V
Junction temperature	-40	125	°C
Storage temperature T_{STG}	-65	150	°C

(1)

(2)

PIN CONFIGURATION



Top View: 20-Lead Plastic QFN 3.5mmx4.5mm

PIN FUNCTIONS

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-20L	UNIT

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft-start and Voltage Tracking						
Power Good Indicator						
Switching Frequency and External Clock Synchronization						
PWM Control						
Bootstrap Diode and Undervoltage Threshold						

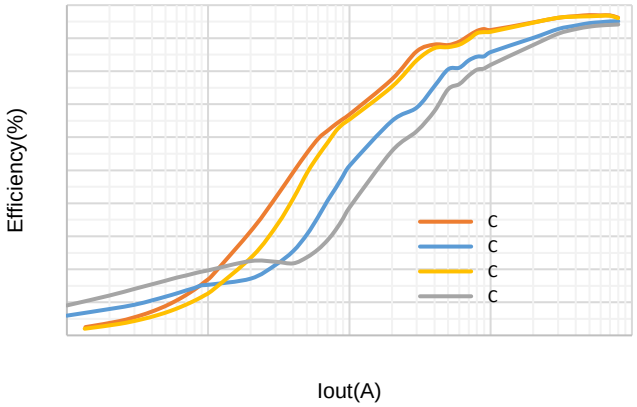
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT

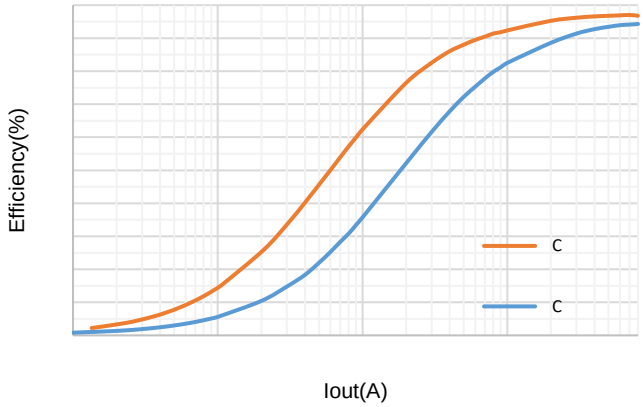
Over Current Protection and Valley Current Limiting

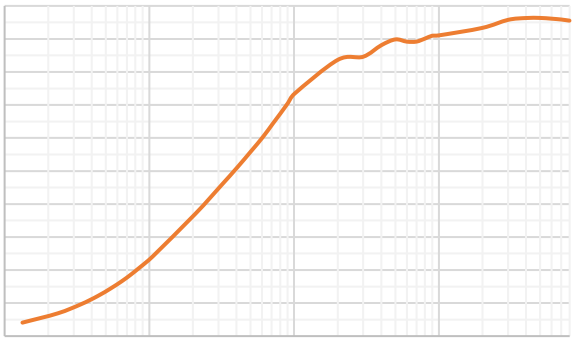
Short Circuit Protection – Duty Cycle ¢ Pro{

046>6<005C600360012>2<00371<0035002E383 31.08 reW* nBT/<002F€ g107-4<004FET1

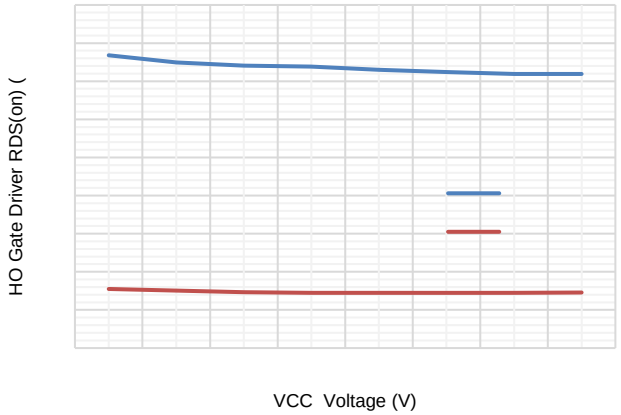
TYPICAL CHARACTERISTICS

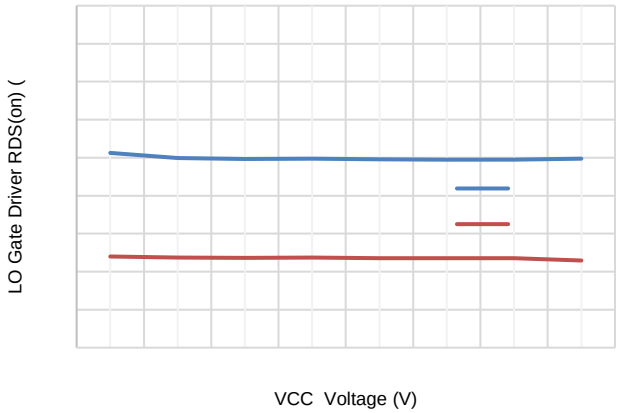


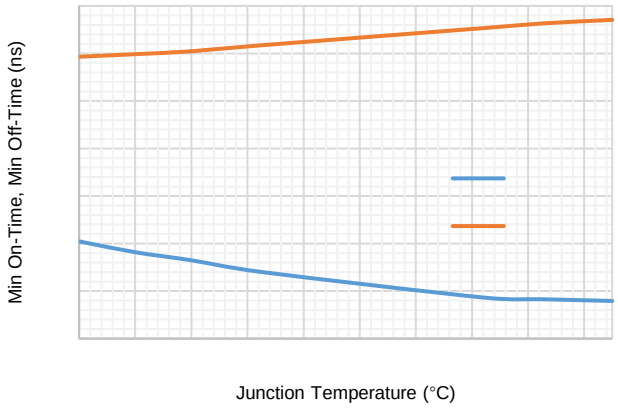


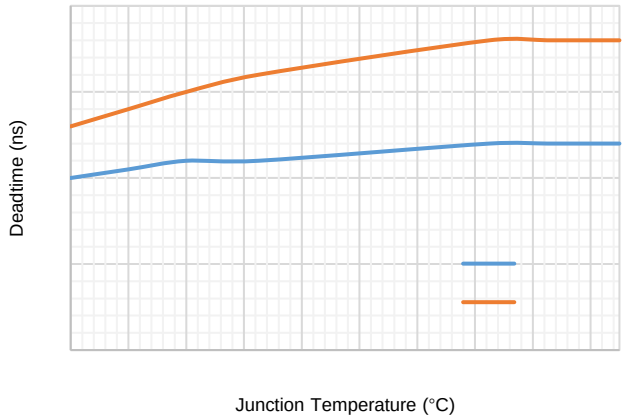


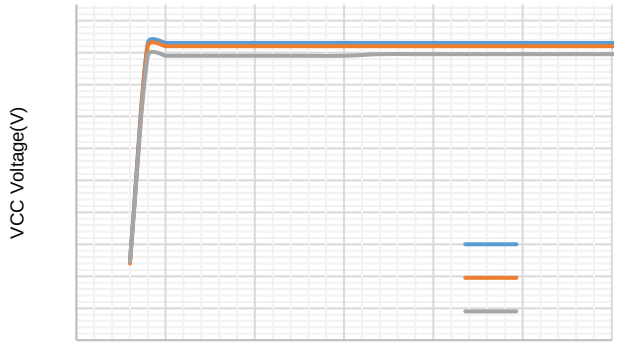
TYPICAL CHARACTERISTICS

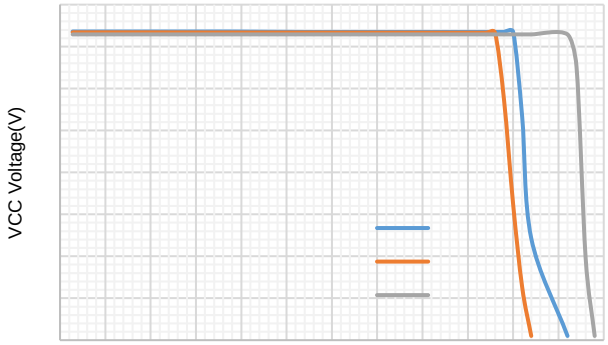




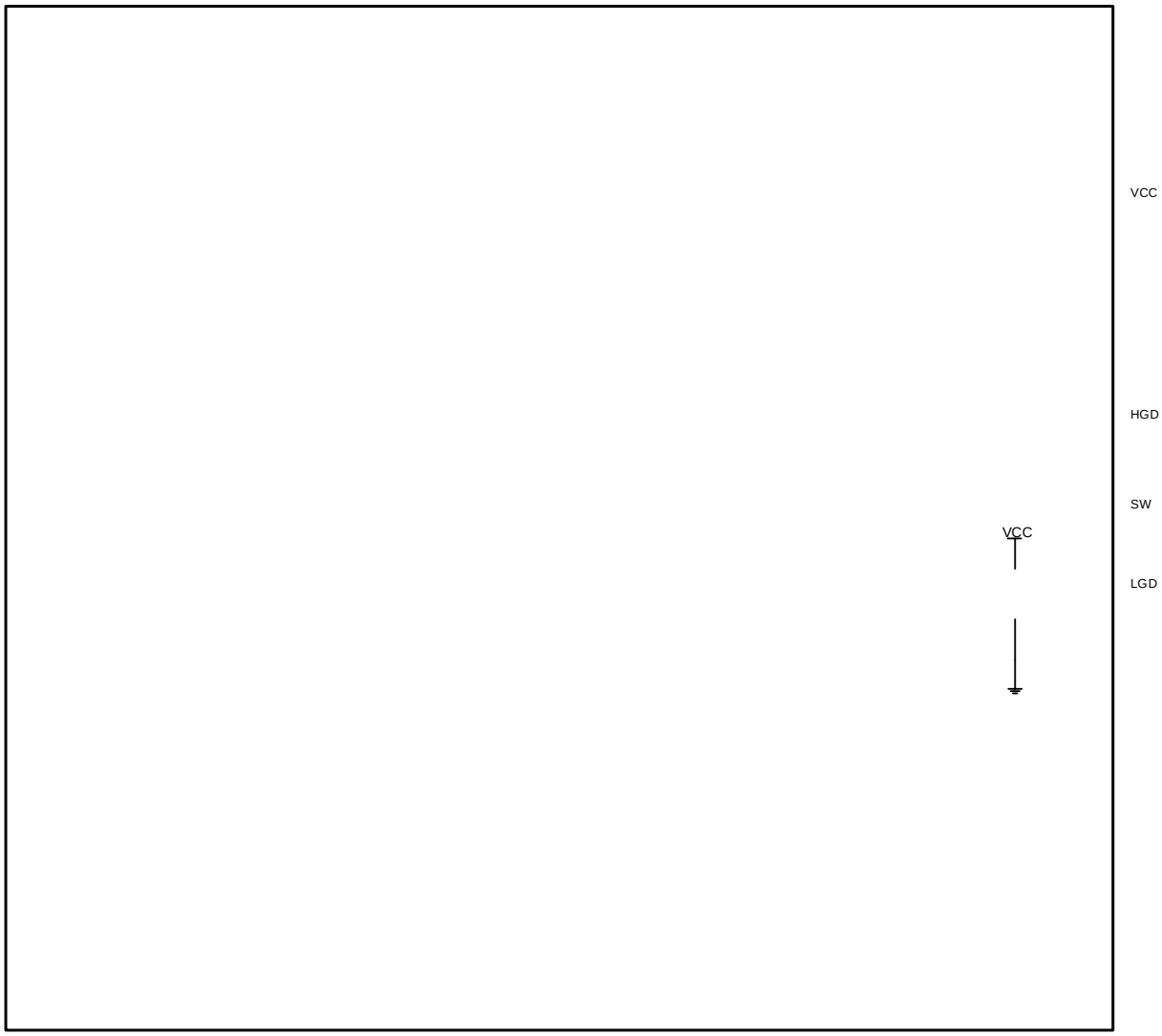








FUNCTIONAL BLOCK DIAGRAM



OPERATION

Overview

It continues to operate during input voltage drops as low as 6 V, at nearly 100% duty cycle if needed, making it an excellent choice for high performance industrial control, robotic, Datacom, and networking communication infrastructure.

The SCT82630 support Forced-PWM (FPWM) and Diode Emulation Mode. FPWM operation eliminates switching frequency variation to minimize EMI, while user selectable diode emulation lowers current consumption at light-load condition. can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications. The device features clock synchronization with clock input and clock output. A 180° out-of-phase clock output relative to the internal oscillator at SYNCOUT configures cascaded or multichannel power supplies to reduce input capacitor ripple current and EMI filter size.

An external voltage or the output of the buck converter itself source can power internal VCC or EXTVCC helping to increase overall efficiency and decrease internal self-heating from power dissipated in the internal VCC LDO even with 5V output voltage.

The SCT82630 features additional features for flexible and robust design including a configurable soft start, an open-drain power-good monitor for fault reporting and output monitoring, monotonic start-up into pre-biased loads, integrated VCC bias supply regulator and bootstrap diode, external power supply tracking, precision enable input with hysteresis for adjustable line under voltage lockout (UVLO), hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

The SCT82630 controller is available in a 4.5-mm × 3.5-mm thermally enhanced, 20-pin QFN package

Input Voltage Range

necessary regulator dropout specification.

Output Voltage Regulation Point and Accuracy

The feedback reference voltage at the FB pin is typical 0.8 V with a feedback system accuracy over the full junction temperature range of ±1%. Junction temperature range for the device is 40°C to +125°C. the SCT82630 is generally capable of providing output voltages in the range of 0.8 V to a maximum of 65V or slightly less than VIN depending on switching frequency and load current levels. The output voltage regulation level during normal operation is set by the feedback resistor network, RFB1 and RFB2, connected to the output and FB pin.

High Voltage Internal VCC Bias Supply Regulator and EXTVCC Auxiliary Supply

Power for the high side and low side MOSFET drivers and most other internal control circuitry is derived from the VCC pin. An internal high-voltage VCC regulator directly to input voltage pin up to 65V. The output of internal VCC regulator is set up 7.5V. When the input voltage is below the VCC set point level, the VCC output tracks V_{IN} with a small voltage drop. Connect a ceramic decoupling

The VCC regulator output has a current limit of 40 mA (minimum). At power up, when the VCC voltage exceeds its rising UVLO threshold of 4.5 V the output is enabled if EN is above 1.2V, and the soft-start sequence begins. The output remains active until the VCC voltage falls below its falling UVLO threshold of typical 4.3 V or if EN goes to a standby or shutdown state.

There are two ways powering the VCC pin with the external source helping to increase overall efficiency and decrease internal self-heating through power dissipated in the LDO. Connecting the output voltage or an auxiliary bias supply rail (up to 13V) to VCC using a diode. Or powering the EXTVCC pin with an external power source or from output voltage directly which is very convenient for customer especially when output voltage is setup at 5V as shown in Figure 20. If the EXTVCC pin is tied to an external source larger than 4.7V, then the internal VCC LDO is shut down and an internal switch shorts the EXTVCC pin to the VCC pin. This external power source could be the output of the buck switching converter itself if the output is programmed to higher than 4.7V.

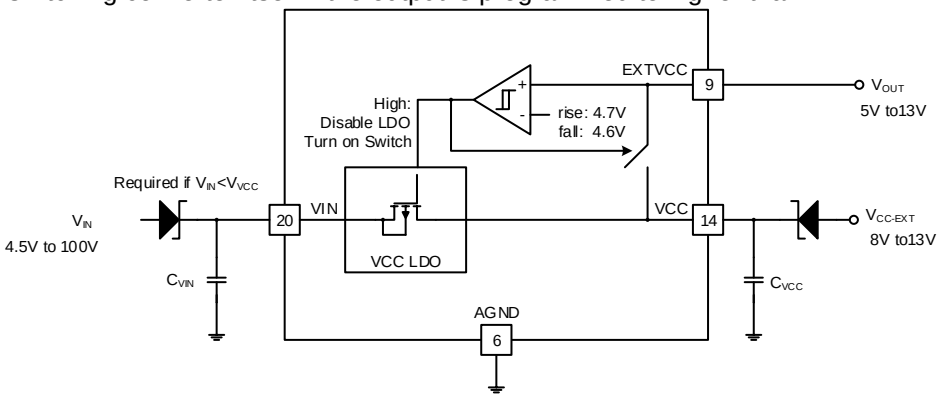


Figure 20. VCC Bias Supply Connecting EXTVCC Auxiliary Supply

Enable and programmable UVLO

The SCT82630 can be shut down using the EN pin. Pulling this pin below 1.2V prevents the controller from switching, and less than 0.41V disables most of the internal bias circuitry, including the VCC regulator. The shutdown IQ is about 7.2

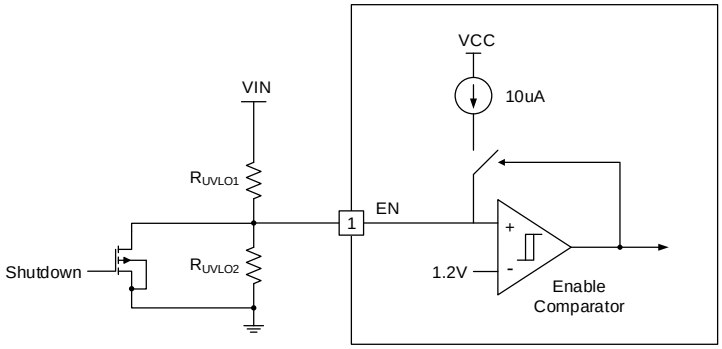


Figure 21. Programmable Input Voltage VIN UVLO Thresholds

Soft Start and Voltage Tracking

The SS/TRK pin voltage controls start-up of output voltage. After the EN pin exceeds its rising threshold of 1.2 V, the SCT82630 begins regulating the output to the level dictated by the feedback resistor network and SS/TRK voltage the soft-start capacitor connecting SS/TRK pin. Soft start avoids inrush current as a result of high output capacitance to avoid an overcurrent condition. The inrush stress on the input supply rail is also reduced. The soft-start time, t_{SS}, for the output voltage to ramp to its nominal level is set by Equation 3.

Where

C_{SS} is the soft-start capacitance

V_{REF} is the 0.8V reference voltage

I_{SS}

Calculate C_{SS} using Equation 4.

The SS/TRK pin is internally clamped to VFB + 115 mV to allow a soft-start recovery from an overload event. The clamp circuit requires a soft-start capacitance greater than 2nF for stability and has a current limit of approximately 2mA.

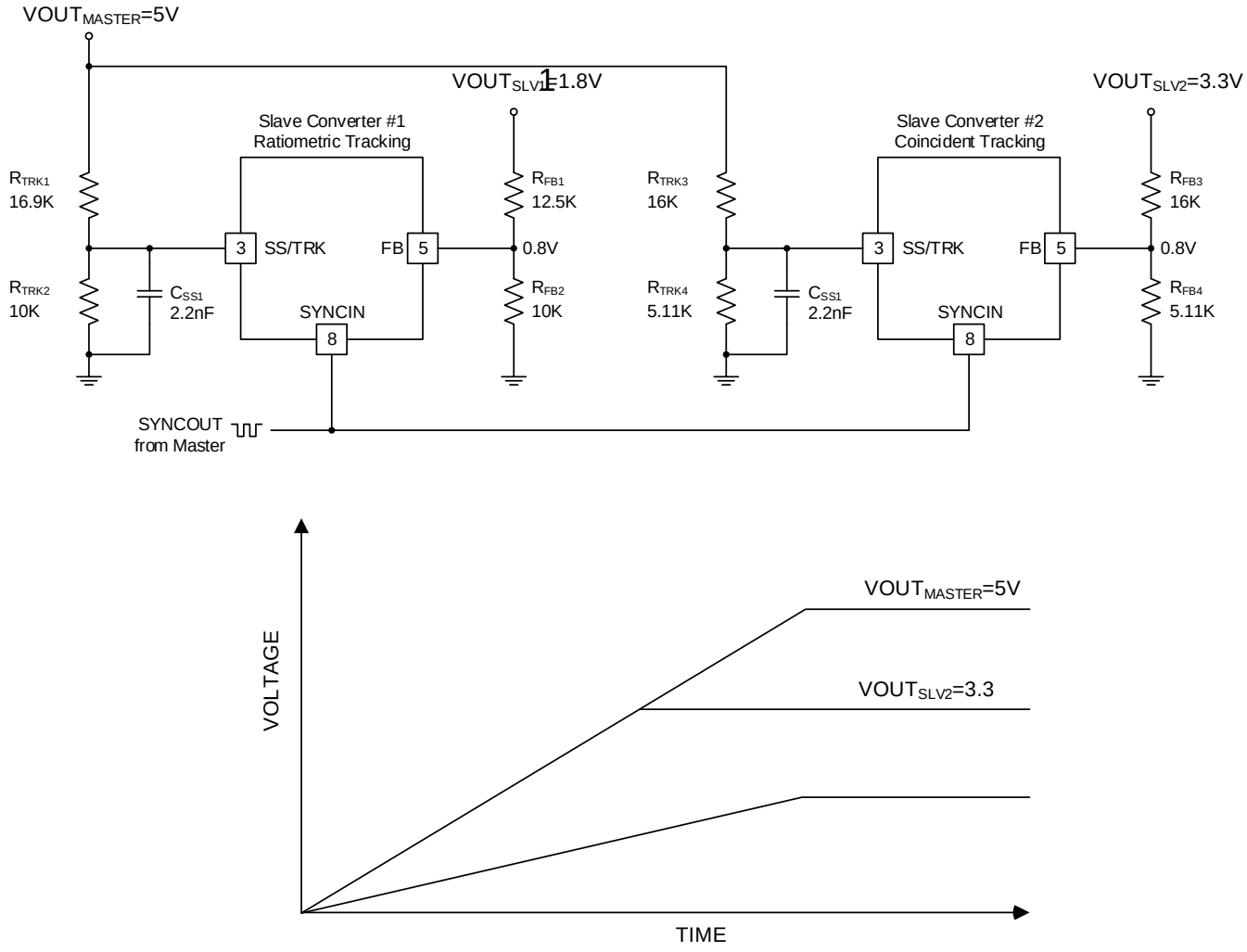
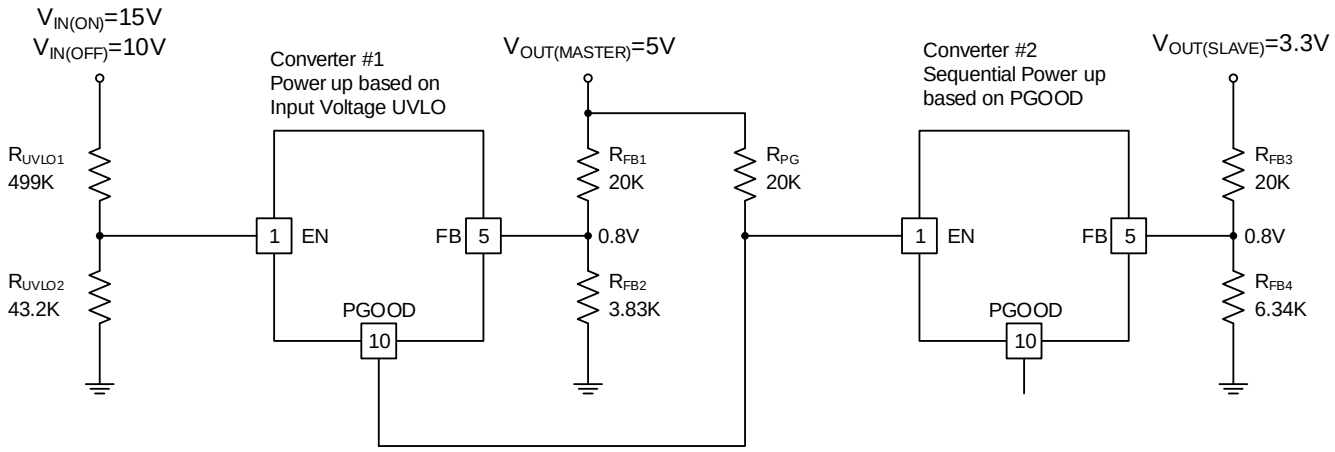


Figure 22. Tracking Implementation with Master, Ratiometric and Coincident Slave Rails

Power Good Monitor PGOOD



Switching Frequency and Clock Synchronization

Switching Frequency (kHz)	Frequency Set Resistance (kΩ)

Clock frequency range: 100 kHz to 1 MHz
Clock frequency: 20% to +50% of the free-running frequency set by R_{RT}
Clock maximum voltage amplitude: 13 V
Clock minimum pulse width: 50 ns

Frequency Spread Spectrum

To reduce EMI, the SCT82630 implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the programmed switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This frequency dithering function is effective for both frequency programmed by resistor placed at RT pin and an external clock synchronization application.

Voltage Mode Control

The SCT82630 incorporates a voltage-mode control loop implementation. The amplitude of PWM triangle wave is larger and the pulse width has better anti-noise margin. The duty cycle adjustment is unrestricted with good response to the change of output load. Input voltage feedforward eliminates the input voltage dependence of the PWM modulator gain. This configuration allows the controller to maintain stability throughout the entire input voltage operating range and provides for optimal response to input voltage transient disturbances. The constant gain provided by the controller greatly simplifies loop compensation design because the loop characteristics remain constant as the input voltage changes, unlike a buck converter without voltage feedforward. An increase in input voltage is matched by a concomitant increase in ramp voltage amplitude to maintain constant modulator gain. The input voltage feedforward gain, KFF, is 12, equivalent to the input voltage divided by the ramp amplitude, VIN/VRAMP.

Gate Drivers

The SCT82630 gate driver impedances are low enough to perform effectively in high output current applications where large die-size or paralleled MOSFETs with correspondingly large gate charge, Q_G, are used. Measured at V_{CC} = 7.5 V, the low-side driver has a low impedance pulldown path of 0.6 effect of dv/dt induced turn-on, particularly with low gate-threshold voltage MOSFETs. Similarly, the high-side pull-up and pulldown impedances, respectively, for faster switching transition times, lower switching loss, and greater efficiency.

The high-side gate driver works in conjunction with an integrated bootstrap diode and external bootstrap capacitor, C_{BST}. When the low-side MOSFET conducts, the SW voltage is approximately at 0V and C_{BST} is charged from VCC citor close to the BST and SW pins.

Furthermore, there is a proprietary adaptive dead-time control on both switching edges to prevent shoot-through and cross-conduction, minimize body diode conduction time, and reduce body diode reverse recovery losses.

Current Sensing and Overcurrent Protection

The SCT82630 implements two lossless current sense schemes in Figure 24, using the on-state resistance of the low-side MOSFET or alternative implementation with current shunt resistor RS, limiting the inductor current during an overload or output short-circuit condition. The controller senses the inductor current during the PWM off-time when LGD is high.

The ILIM pin sources a reference current that flows in an external resistor, designated RILIM, to program of the current limit threshold. A current limit comparator on the ILIM pin prevents further SW pulses if the ILIM pin voltage goes below GND.

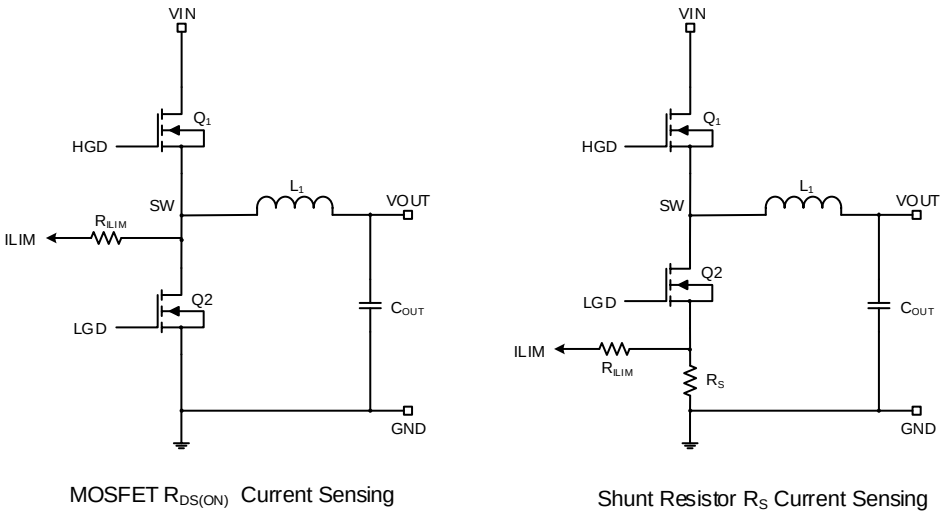


Figure 24. Current Sensing Schemes

Two optional connections sensing inductor current:

$R_{DS(on)}$ sensing mode: R_{ILIM} is tied to SW to use the RDS(on) of the low-side MOSFET as a sensing element.

R_{SENSE} shut mode: R_{ILIM} is tied to a shunt resistor connected at the source of the low-side MOSFET.

The SCT82630 detects the appropriate mode at start-up and sets the source current amplitude and temperature coefficient (TC) accordingl

Device Functional Modes

Shutdown Mode

The EN pin provides ON / OFF control for the SCT82630. When the EN voltage is below 0.38V typical, the device is in shutdown mode. Both the internal bias supply LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 7.2 SCT82630 also includes under voltage protection of the internal bias LDO. If the internal bias supply voltage is below its UVLO threshold level, the switching regulator remains off.

Standby Mode

The internal bias supply LDO has a lower enable threshold than the switching regulator. When the EN voltage exceeds 0.41 V typical and is below the precision enable threshold 1.2 V typically, the internal LDO is on and regulating. Switching action and output voltage regulation are disabled in standby mode.

Active Mode

The SCT82630 is in active mode in7(he)4( )-22(d)-(n7()-119CCd)-(n8ol)7(t)-10(a)-9(geg-1 26.5 4-5( )-107(i)-6(nl)-4(e)5(d)-9( )

Control loop compensation

The SCT82630 integrates the voltage mode control loop implementation and feeds the input voltage forward to eliminate the input voltage dependence of the PWM modulator gain. The voltage mode buck control loop is show as below:

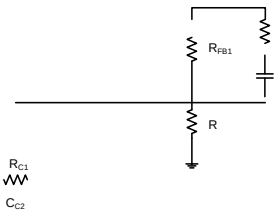


Figure 25. Buck circuit voltage loop control diagram

The compensation network typically employed with voltage-mode control is a Type-III circuit with three poles and two zeros. One compensator pole is locaten0 G27833 170.81e3com 1putB0000091 34ori7(nd)i(es)-2 rett 34ntor4 17andQ EMC

Duty-cycle-to-output transfer function	$G_{vd}(s) \quad \frac{V_o(s)}{d(s)} \quad V_{IN} \frac{1 \quad \frac{s}{Z_{ESR}}}{1 \quad \frac{s}{Q_o \quad o} \quad \frac{s^2}{Z \quad ^2_o}}$
Compensator transfer function	$G_C(s) \quad \frac{V_{comp}(s)}{V_o(s)} \quad \frac{1}{R_{FB1}C_{C1}s} \frac{\S 1 \quad \frac{s}{z1}\S \quad 1 \quad \frac{s}{Z \quad i_{z2}}}{\S 1 \quad \frac{s}{p1}\S \quad 1 \quad \frac{s}{Z \quad i_{p2}}}$
Modulator transfer function	$F_m \quad \frac{d(s)}{V_{comp}(s)} \quad \frac{1}{V_{ramp}}$

The compensation network typically employed with voltage-mode control is a Type-III circuit with three poles and two zeros. One compensator pole is located at the origin to realize high DC gain. The normal compensation strategy uses two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero, with the remaining compensator pole located at one-half switching frequency to attenuate high frequency noise. The resistor divider network to FB determines the desired output voltage. Note that the lower feedback resistor, R_{FB2} , has no impact on the control loop from an AC standpoint because the FB node is the input to an error amplifier and is effectively at AC ground. Hence, the control loop is designed irrespective of output voltage level. The proviso here is the necessary output capacitance derating with bias voltage and temperature. The poles and zeros(no include original pole) inherent to the power stage and compensator are respectively illustrated by red and blue dashed rings in the schematic embedded in Table 3.

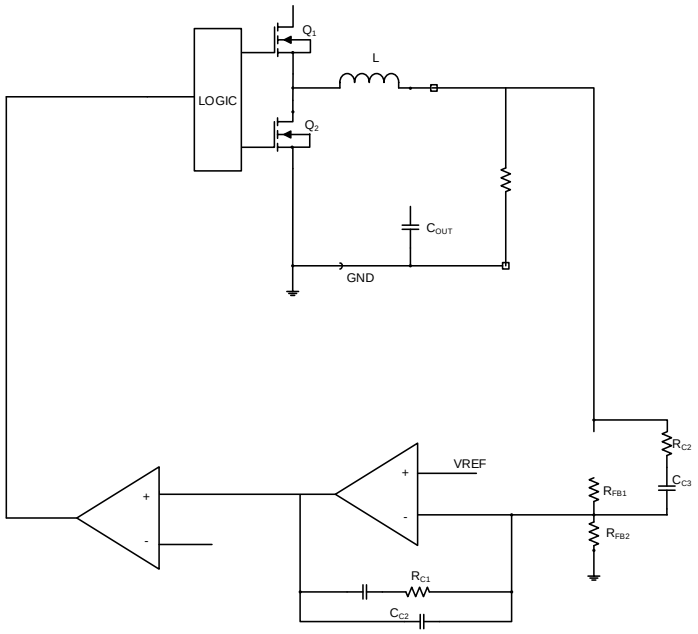


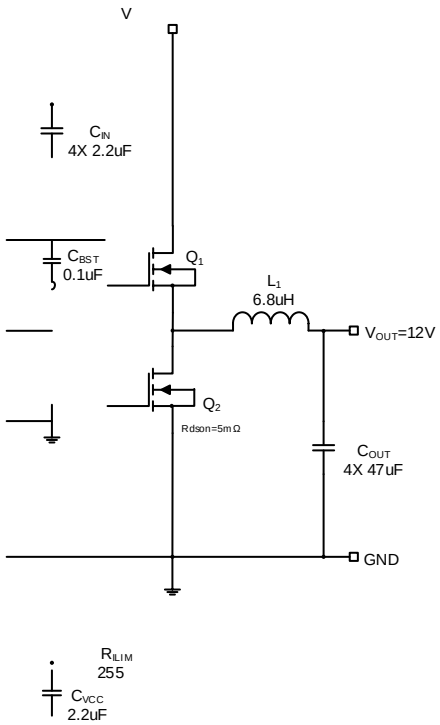
Figure 26. Control loop with poles and zeros

$\omega_{z1} = K \cdot \omega_o$, $\omega_{z2} = \omega_o$, $\omega_{p1} = \omega_{SW/2}$, $\omega_{p2} = \omega_{ESR}$

$R_{FB2} \quad \frac{R_{FB1}}{V_{OUT} / V_{REF} \quad 1}$	$C_{C1} \quad K_{FF} / \ 2\mathcal{S} f_c \ R_{FB1} \ K)$
$R_{C1} \quad \frac{1}{K \ Z_o \tilde{} \ C_{C1}}$	$C_{C2} \quad \frac{1}{Z_{p1} \tilde{} R_{C1}}$
$R_{C2} \quad \frac{Z_0}{ESR \ Z \ _0} \ R_{FB1}$	$C_{C3} \quad \frac{1}{ESR \ R_{C2}}$

APPLICATION INFORMATION

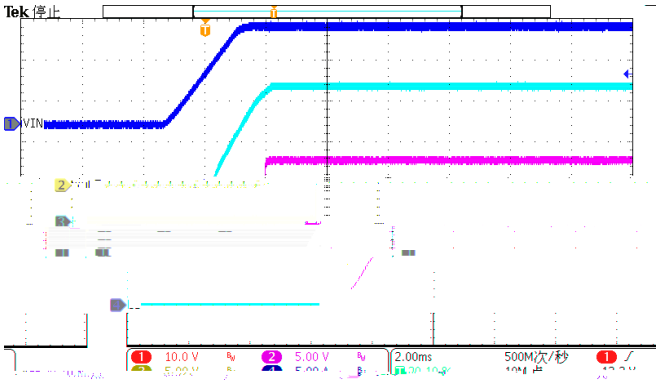
Typical Application

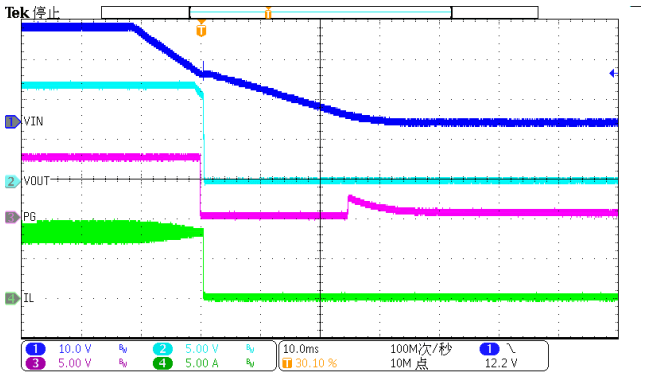


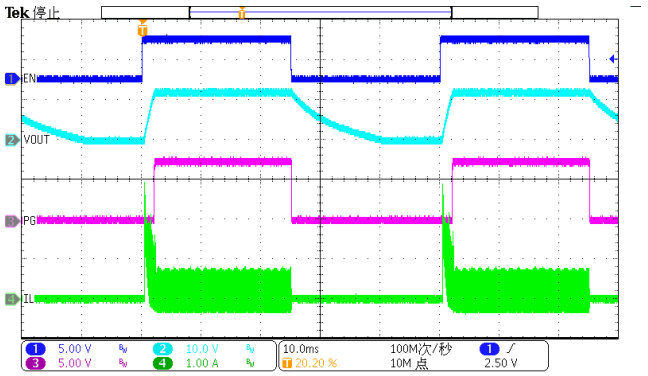
Design Parameters

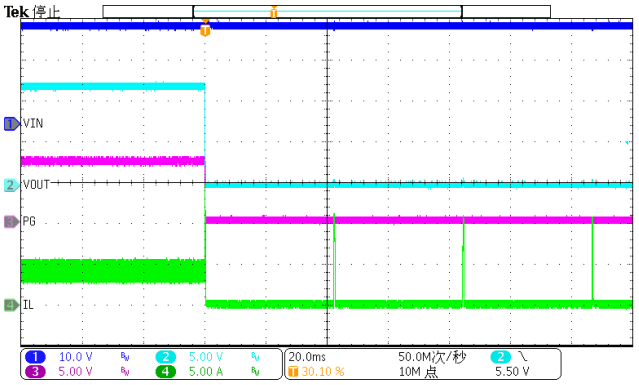
Design Parameters	Example Value

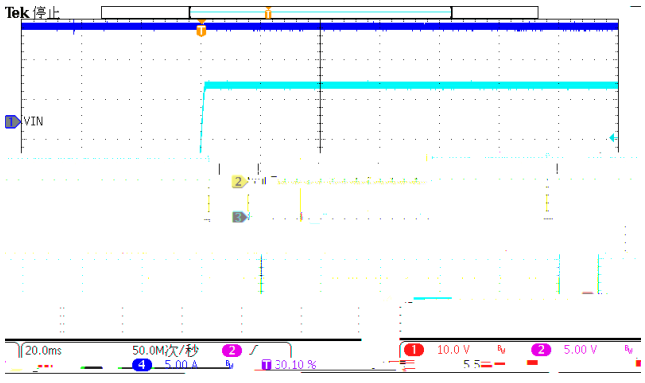
Application Waveforms











Application Waveforms(continued)

Typical Application

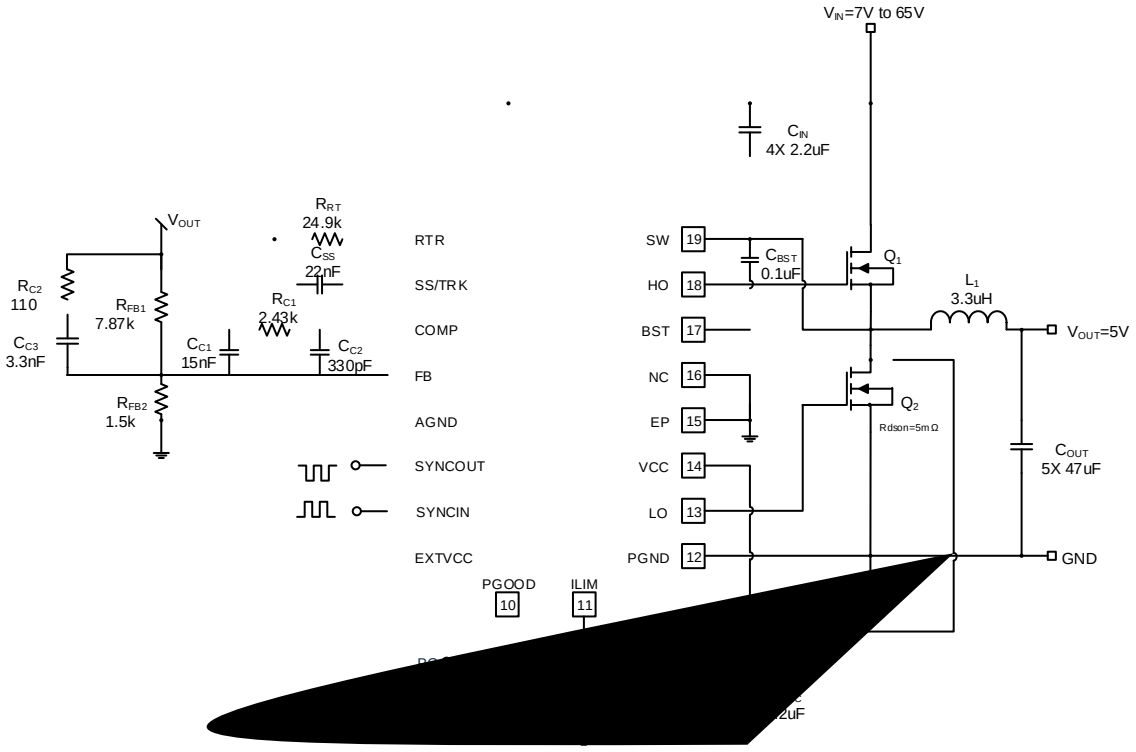
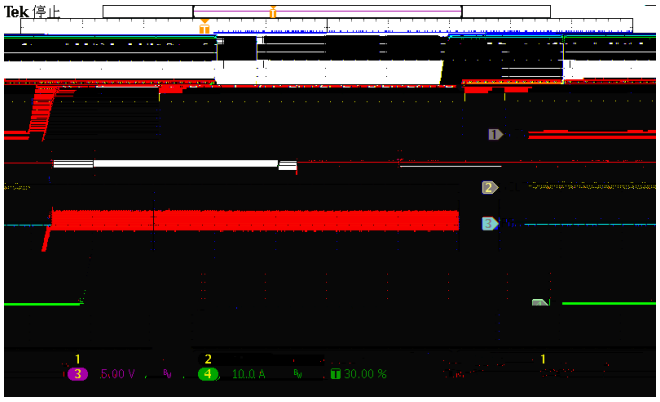


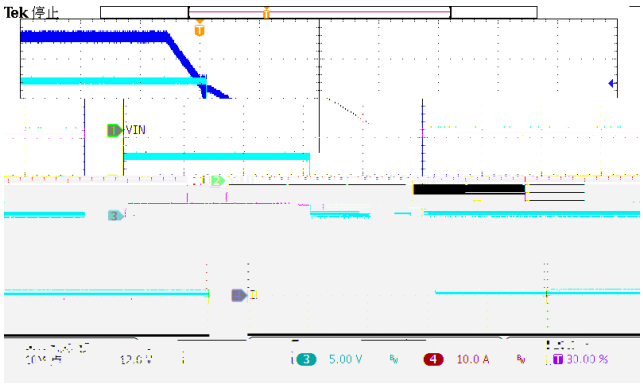
Figure 41. Application Schematic, 24V to 5V, 20A Buck Regulator at 400kHz

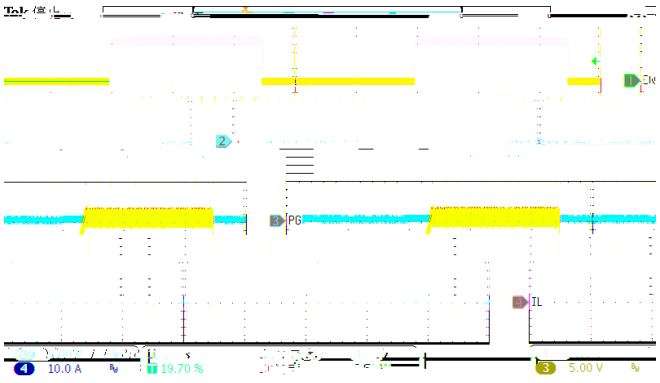
Design Parameters

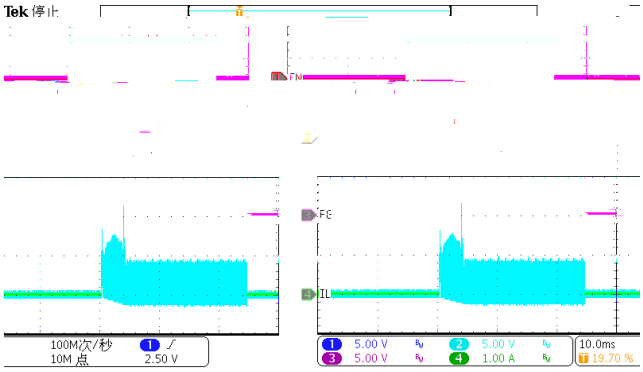
Design Parameters	Example Value

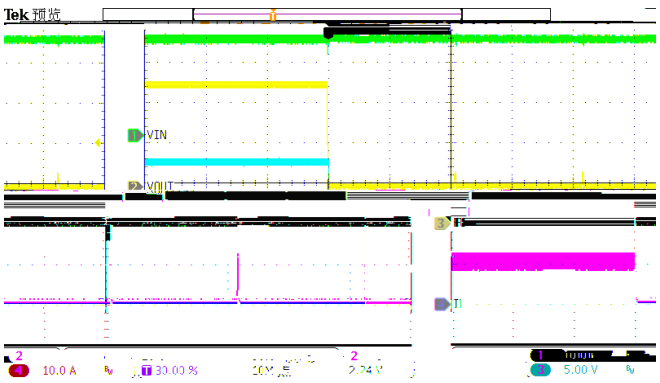
Application Waveforms

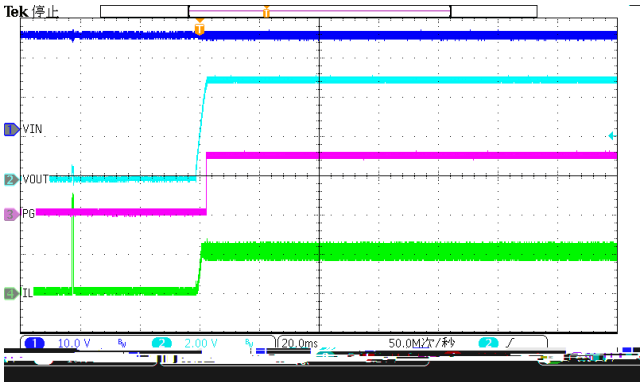




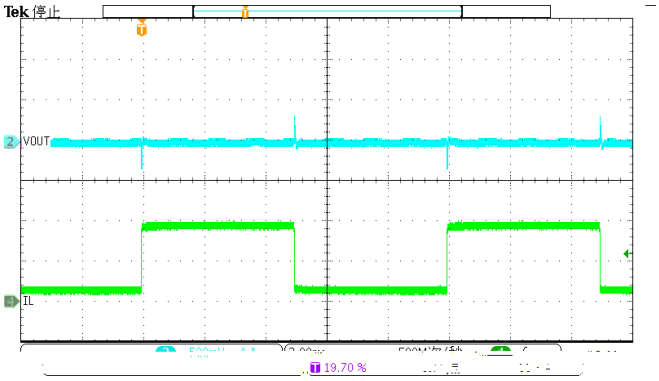


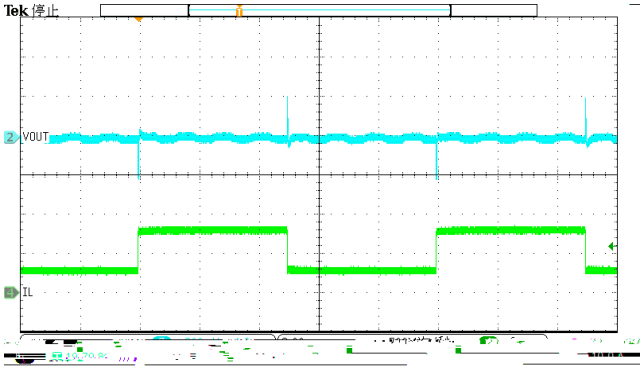


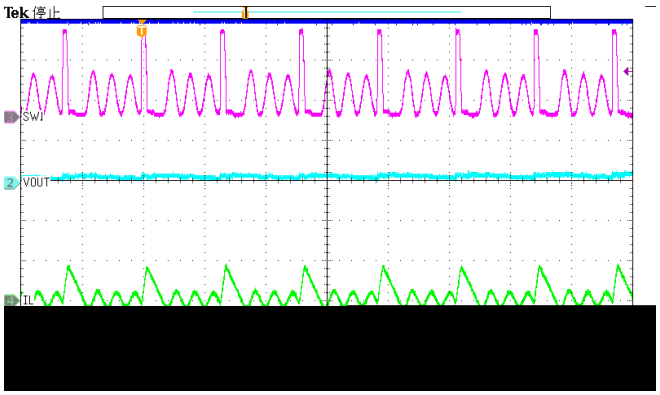


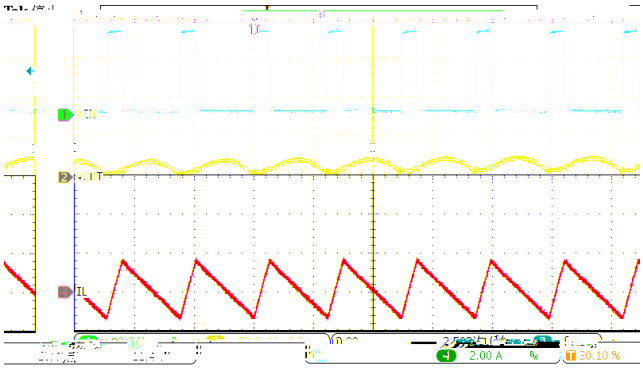


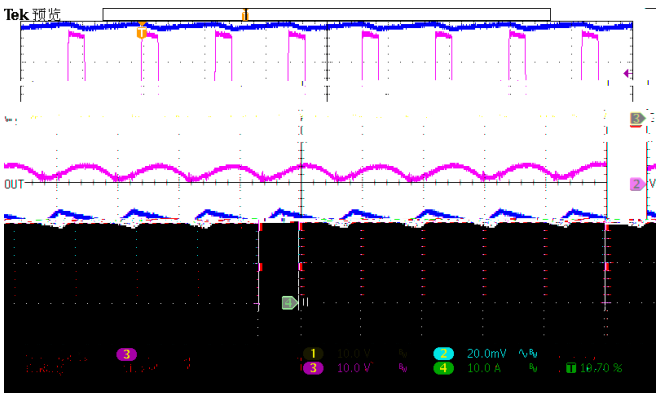
Application Waveforms(continued)











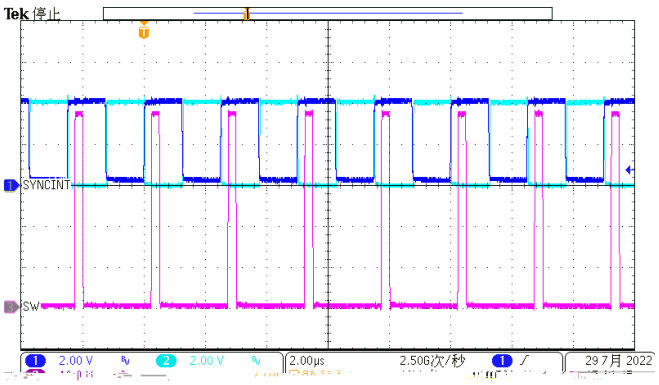
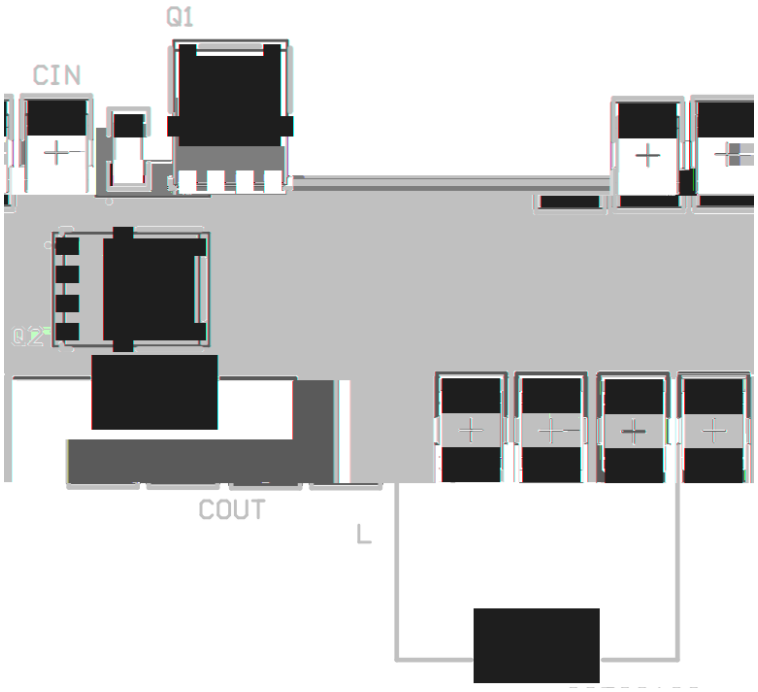
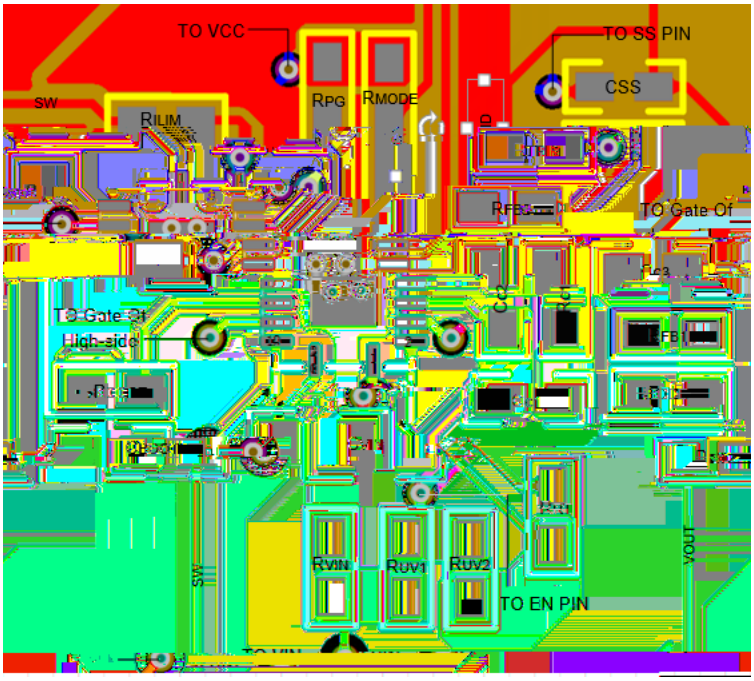


Table 5: Compensation Values for Typical Output Voltage/Capacitor Combinations at fsw=400KHz

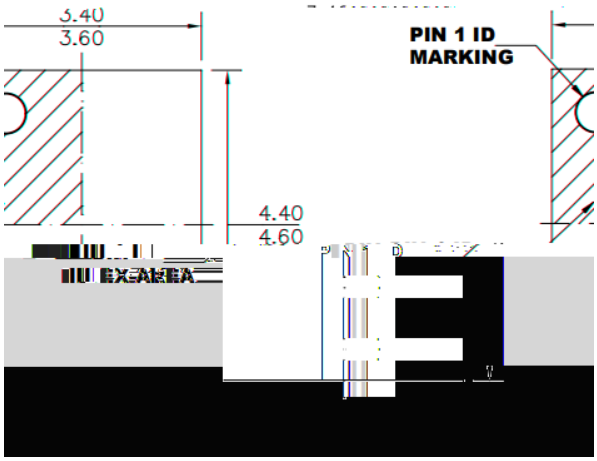
		O							

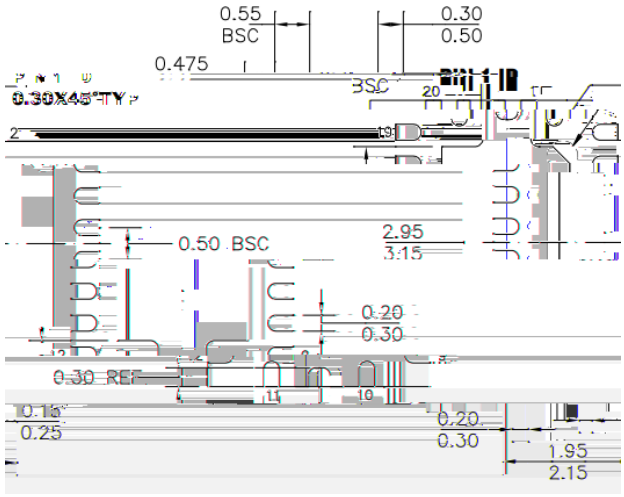
Layout Guideline

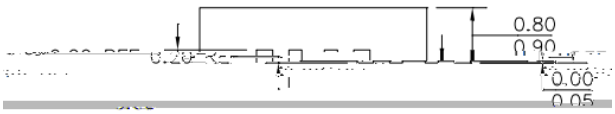


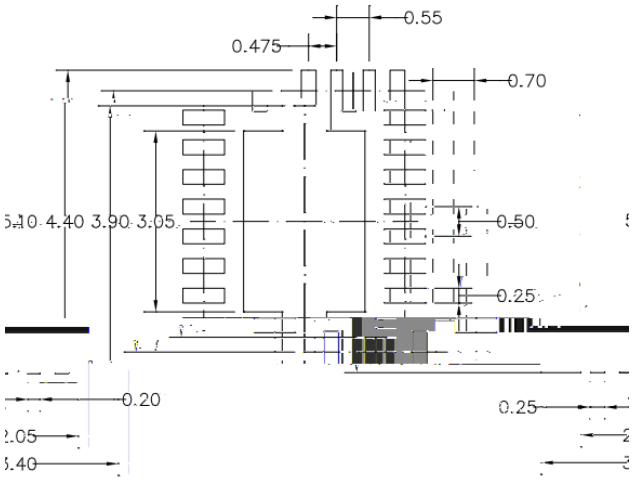

TO VCC
TO SS PIN
CSS
SW
RILIM
RPG
RMODE
RFB3
TO Gate Of
TO Gate Of
High-side
RVIN
RUV1
RUV2
VOUT
TO EN PIN

PACKAGE INFORMATION









NOTE:

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4.
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TAPE AND REEL INFORMATION