NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production.

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT52245STD	2245	SOP-8

Over operating free-air temperature range unless otherwise noted

(APTAET 9Tf1 001 5

V_{DD}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{DD}	Operating supply voltage		4.5		24	V
V_{DD_UVLO}	Input UVLO Hysteresis	V_{DD} rising		4.2 300	4.5	V mV
I_Q	Supply current	V_{DD}=12V, INA- =INB =GND		130		uA
		V_{DD}=12V, INA- =INB =12V		190		uA
INPUTS						
V_{INA-,INB_H}	Input logic high threshold Output low for inverting input Output high for non-inverting input			2.1	2.4	V
V_{INA-,INB_L}	Input logic low threshold Output high for inverting input Output low for non-inverting input		0.8	1		V
V_{IN_Hys}	Hysteresis			1.1		V
OUTPUTS						
$V_{DD}\_V_{OH}$	Output output high voltage	I_{OUT}= - 10mA			150	mV
V_{OL}	Output low voltage	I_{OUT}= 10mA			10	mV
$I_{SINK/SRC}$	Output sink/source peak current	C_{Load}=10nF, F_{SW}=1kHz		4		A
R_{OH}	Output pull high resistance (only PMOS ON)	I_{OUT}= - 10mA	5	9	18	
R_{OL}	Output pull low resistance	I_{OUT}= 10mA	0.3	0.6	1.2	
Timing						
T_R	Output rising time	C_{Load}=1nF		8	20	ns
T_F	Output falling time	C_{Load}=1nF		8	20	ns
T_{D_IN}	Input to output propagation delay, Rising edge			13	25	ns
	Input to output propagation delay, Falling edge			13	25	ns
T_{MIN_ON}	Minimum input pulse width	C_{Load}=1nF		20	30	ns
Protection						
T_{SD}	Thermal shutdown threshold*	T_J rising		170		°C
	Hysteresis			25		°C

*Derived from bench characterization

V_{IN}=12V, T_A= 25°C.

Figure 1. UVLO vs Temperature

Figure 2.

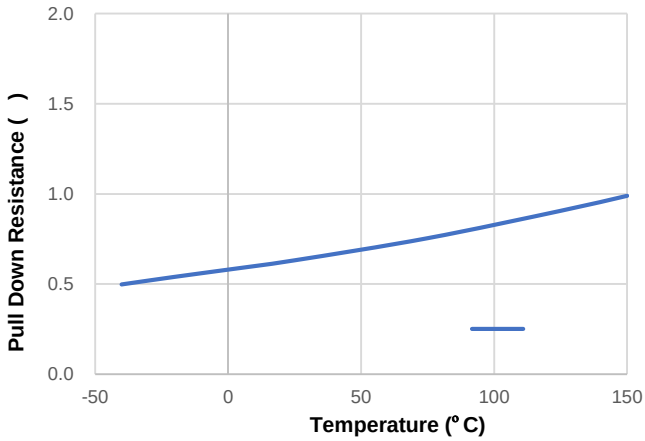


Figure 7. ROL vs Temperature

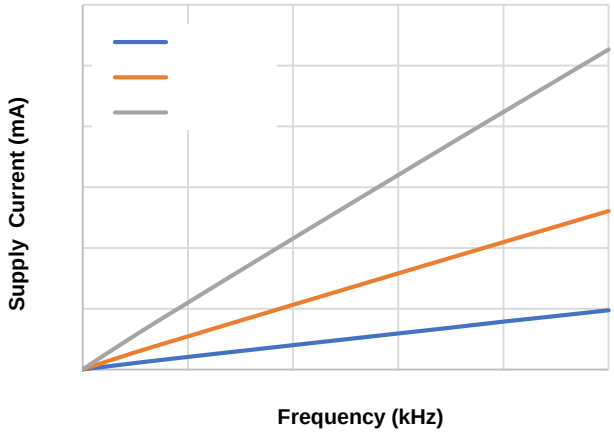


Figure 8. Operation Supply Current vs Frequency, C_{OUT}=1nF

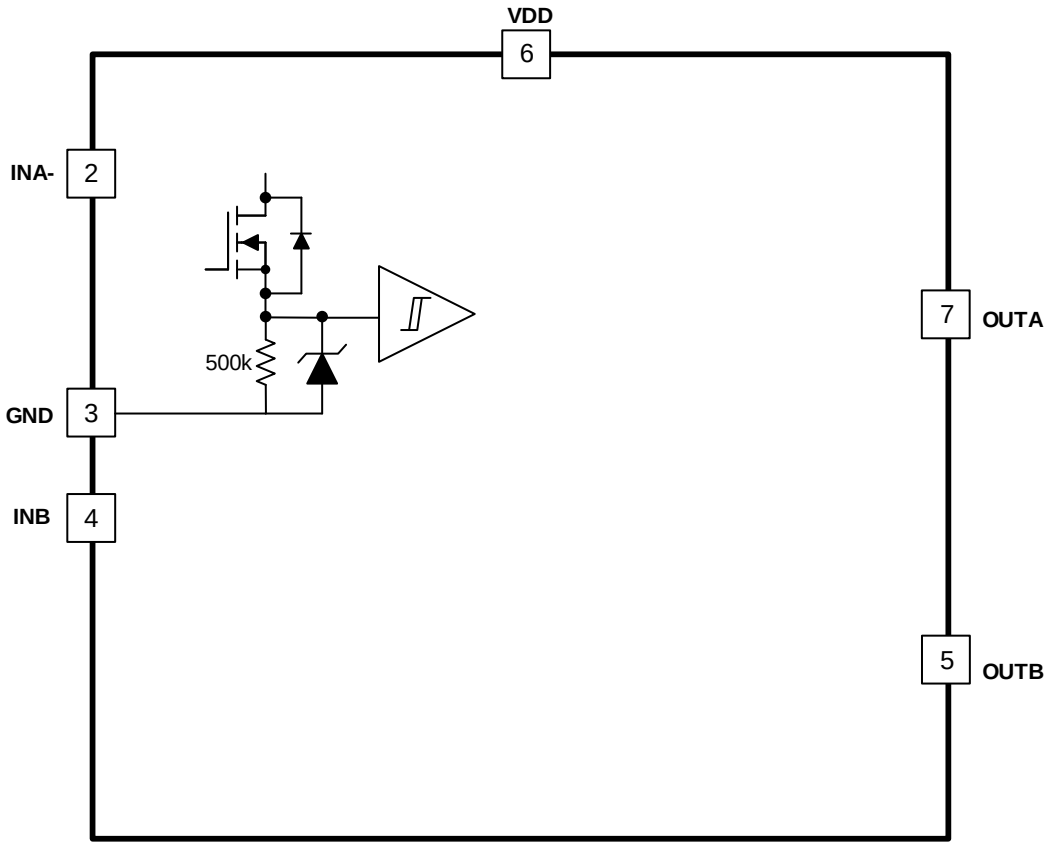


Figure 9. Functional Block Diagram

Overview

The SCT52245 is a dual-channel high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with the minimum propagation delay 13ns from input to output. The ability to handle -5V DC input increases the noise immunity of driver input stage, the 24V rail-to-rail output improves the SCT52245 output stage robustness during switching load fast transition. Table 1 shows the device output logic truth table.

Table 1: the SCT52245 Device Logic.

INA-	INB	OUTA	OUTB
L	L	H	L
L	H	H	H
H	L	L	L
H	H	L	H
Any(UVLO)	Any(UVLO)	H	L
Floating	Floating	H	L
L	L	H	L
L	H	H	H
H	L	L	L
H	H	L	H

VDD Power Supply

The SCT52245 operates under a supply voltage range between 4.5V to 24V. For the best high-speed circuit performance, two VDD bypass capacitors in parallel are recommended to prevent noise problems on supply VDD. A 0.1- F surface mount ceramic capacitor must be located as close as possible to the VDD to GND pins of the SCT52245. In addition, a larger capacitor (such as 1- F or 10uF) with relatively low ESR must be connected in parallel, in order to help avoid the unexpected VDD supply glitch. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

Under Voltage Lockout (UVLO)

SCT52245 device Under Voltage Lock Out (UVLO) rising threshold is typically 4.2 V with 300-mV typical hysteresis. When VDD is rising and the level is still below UVLO threshold, OUTB holds the output low regardless of the status of the inputs and OUTA holds the output high regardless of the status of the inputs. The hysteresis prevents output bouncing when low VDD supply voltages have noise from the power supply.

Input Stage

The input of SCT52245 is compatible on TTL input-threshold logic that is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5V. SCT52245 also features tight control of the input pin threshold voltage that ensures stable operation

across temperature. The very low input parasitic capacitance on the input pins increases switching speed and reduces the propagation delay.

Output Stage

The SCT52245 output stage features the pull up structure with P-type MOSFET PM1 and N-type MOSFET NM1 in parallel, as shown in Figure 12. PM1 provides the pull up capability when OUT approaches VDD and the NM1 holds off state, which guarantees the driver output is up to VDD rail. The measurable on-resistance R_{OH} in steady state is the conduction resistance of PM1. NM1 provides a narrow instant peak sourcing current up to 4A to eliminate the turn on time and delay. During the output turn on transition, the equivalent hybrid pull on transient resistance is $1.5R_{OL}$, which is much lower than the DC measured R_{OH}.

The N-type MOSFET NM2 composes the output stage pull down structure; the R_{OL} is the DC measurement and represents the pull down impedance. The output stage of SCT52245 provides rail-to-rail operation, and is able to supply 4A sourcing and 4A sinking peak current. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots. The outputs of the dual channel drivers are designed to withstand 500-mA reverse current without either damaging the device or logic malfunction.

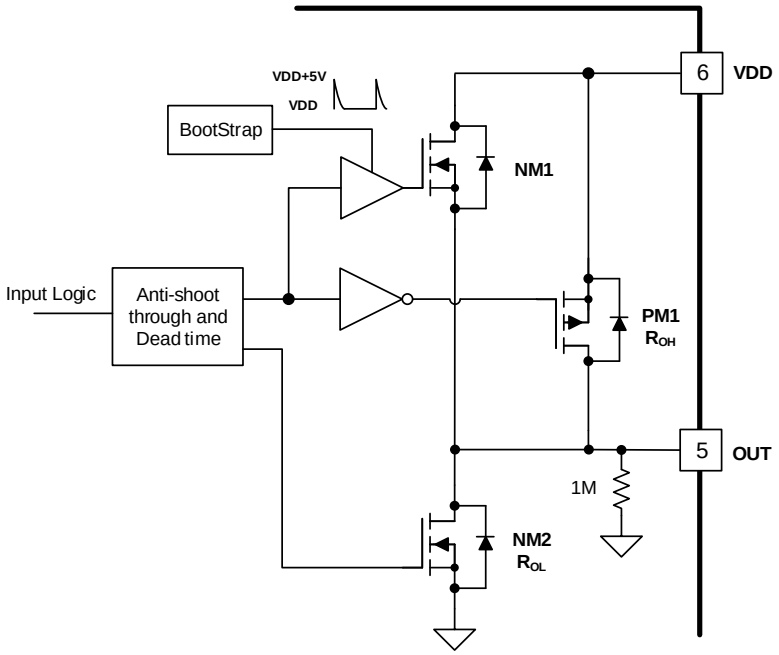


Figure 10. SCT52245 Channel-B Output Stage

Thermal Shutdown

Once the junction temperature in the SCT52245 exceeds 170° C, the thermal sensing circuit stops switching until the junction temperature falling below 145° C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application

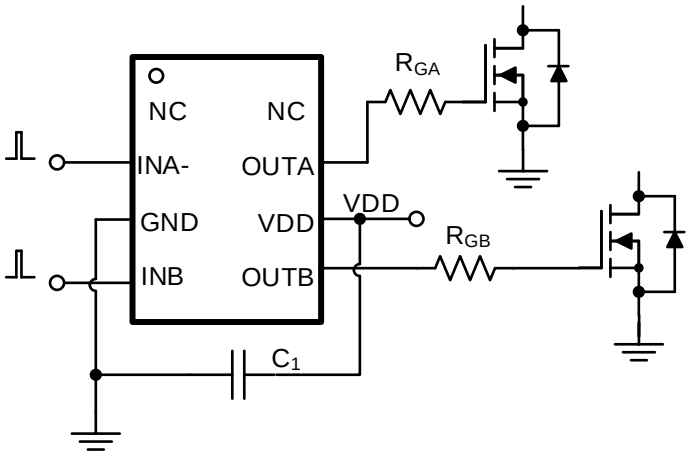


Figure 11. Dual Channel Driver Typical Application

Driver Power Dissipation

Generally, the power dissipated in the SCT52245 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52245 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

Where

- R_{OH} is the equivalent pull up resistance of SCT52245
- R_{OL} is the pull down resistance of SCT52245
- R_G is the gate resistance between driver output and gate of power device.

Application Waveforms

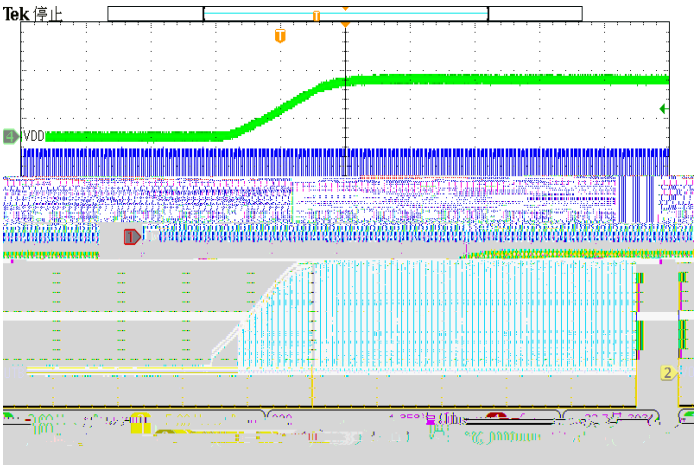


Figure 12. VDD Power ON

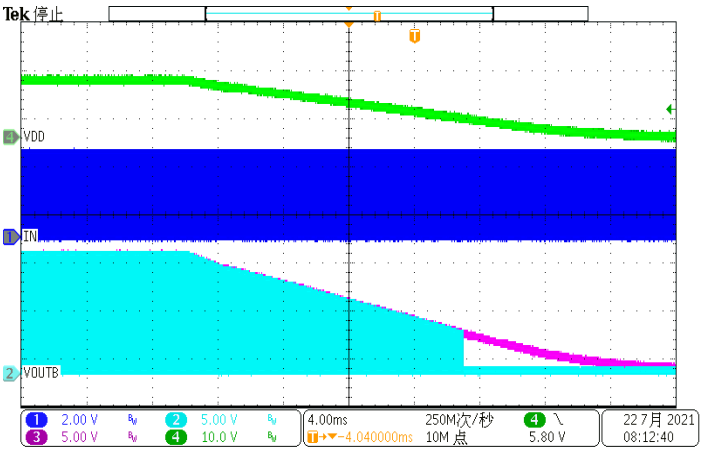


Figure 13. VDD Power OFF

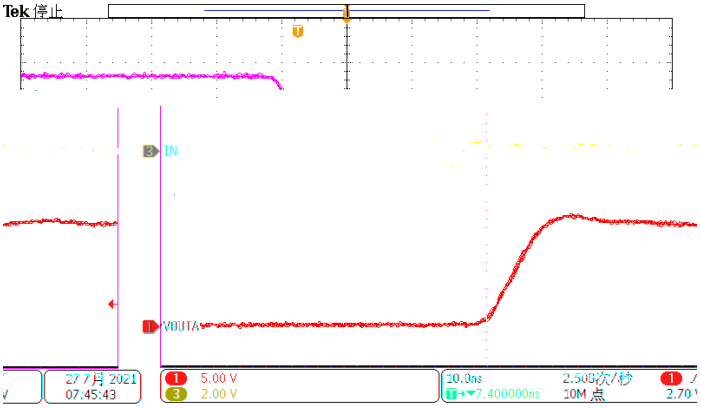


Figure 14. OUTA Switching Rise (C = 1)

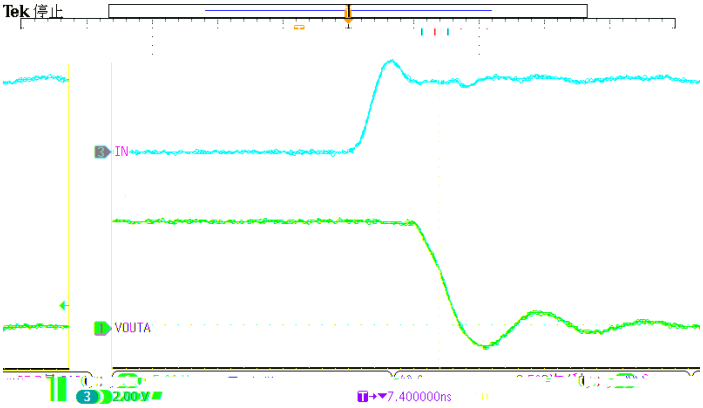


Figure 15. OUTA Switching Fall (C = 1)

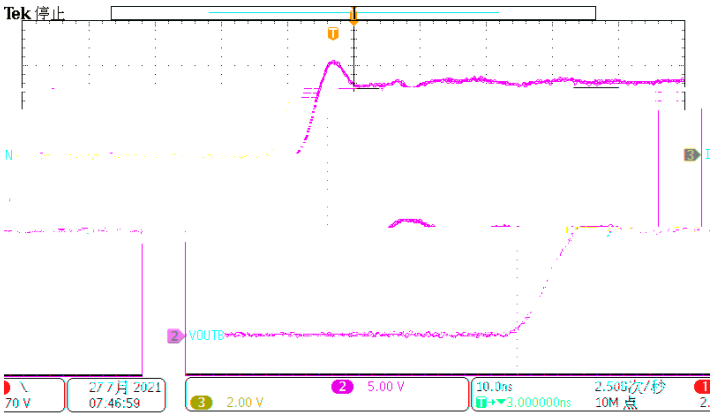


Figure 16. OUTB Switching Rise (C = 1)

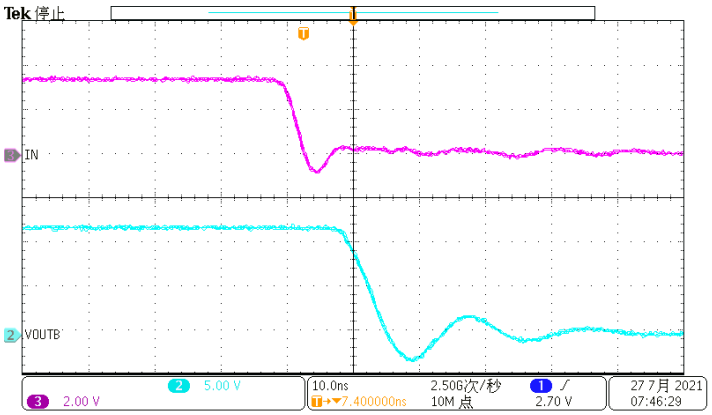


Figure 17. OUTB Switching Fall (C = 1)

Layout Guideline

The SCT52245 provides the 4A output driving current and features very short rising and falling time at the power devices gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not designed well. The regulator could suffer from malfunction and EMI noise problems if the power device gate has serious ringing. Below are the layout recommendations with using SCT52245 and Figure 18 is the layout example.

Put the SCT52245 as close as possible to the power device to minimize the gate driving loop including the driver output and power device gate. The power supply decoupling capacitors needs to be close to the VDD pin and GND pin to reduce the supply ripple.

Star-point grounding is recommended to minimize noise coupling from one current loop to the other. The GND of the driver connects to the other circuit nodes such as source of power MOSFET or ground of PWM controller at single point. The connected paths must be as short as possible to reduce parasitic inductance. A ground plane is to provide noise shielding and thermal dissipation as well.

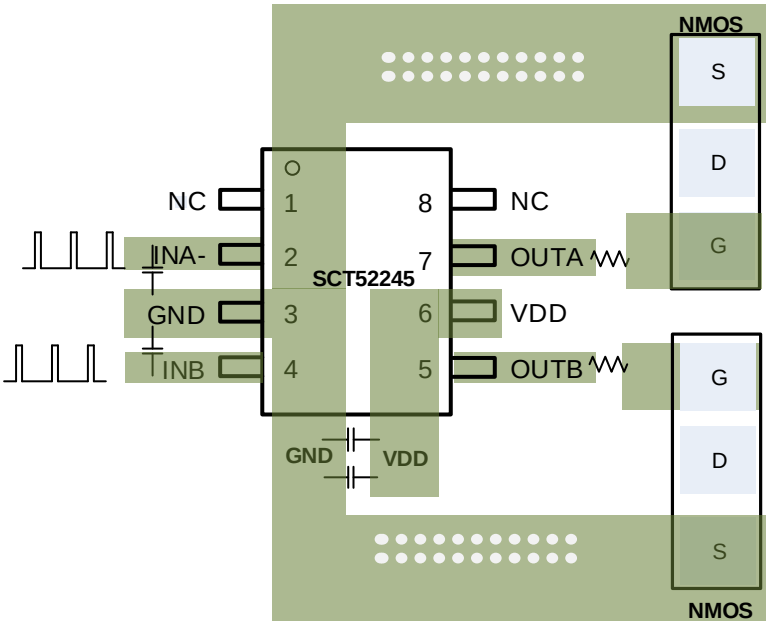


Figure 18. SCT52245 PCB Layout Example

Thermal Considerations

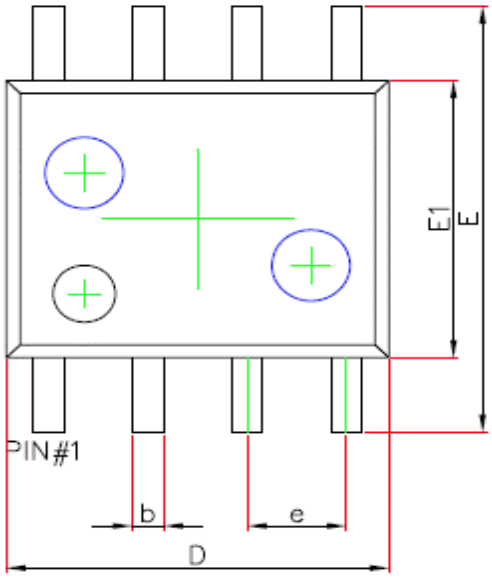
The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (4).

(4)

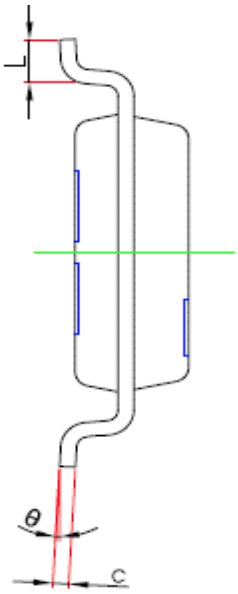
where

- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

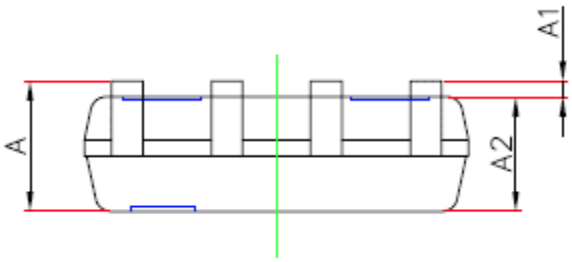
The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, and environmental factor. Soldering the ground pin to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	1.45	---	1.75
A1	0.1	---	0.25
A2	1.35	---	1.55
b	0.33	---	0.51
c	0.17	---	0.25
D	4.7		5.1
E	5.8		6.2
E1	3.8		4.0
e	1.27BSC		
L	0.4		1.27
	0°		8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.