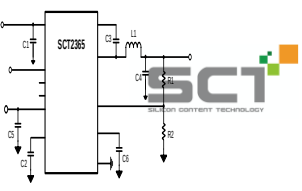
-
-
-
-

-
-
-
-

-
-
-
-

-
-
-
-


SCT2365
C1
C3
L1
C4
R1
R2
C5
C2
C6

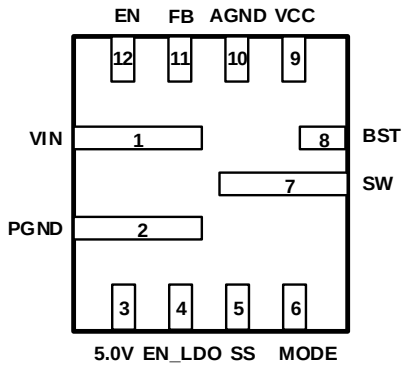
1)

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	32	V
SW	-1	32	V
BST	-0.3	38	V
BST-SW	-0.3	6	V
VOUT	-0.3	16	V
5.0V, EN_LDO, MODE, VCC, FB	-0.3	6	V
Operating junction temperature(2)	-40	125	C
Storage temperature T_{STG}	-65	150	C

(1)

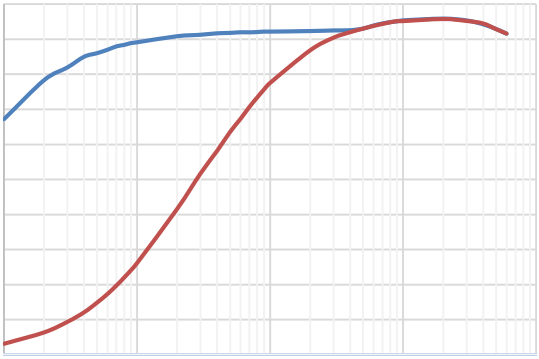
(2)

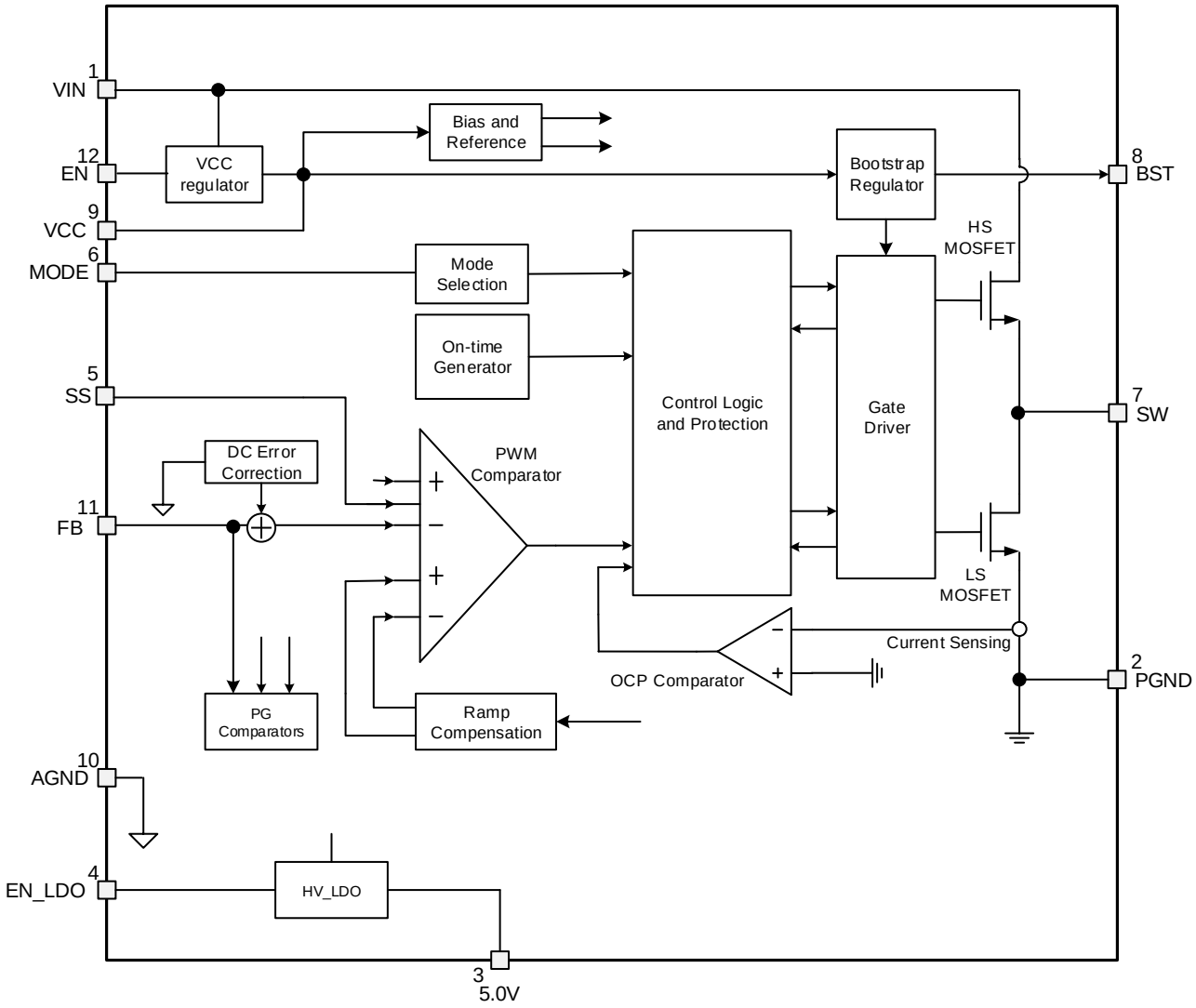


Top View: QFN-12L 3mm x 3mm, Plastic

VIN	1	Input voltage. Decouple the input rail with at least a 0.1uF and 10uF input ceramic capacitor. Place the capacitor as close to VIN and PGND pins as possible. Use wide PCB traces and multiple vias to make the connection.
PGND	2	Power ground. Using wide PCB traces and multiple vias large enough to handle the load current.
5.0V	3	The output of the 5.0V, 150mA LDO output, at least a 4.7uF ceramic cap connected between VCC pin and ground.
EN_LDO	4	

SW	7	Switch output. SW is driven up to VIN through the high-side power MOSFET during on-time. The inductor current drives SW to negative voltage through low-side power MOSFET during off-time. Use wide and short PCB traces to make the connection. Keep the SW pattern area minimized.
BST	8	Bootstrap. Must connect a 0.1uF capacitor or greater between SW and BST to form a floating supply across the gate driver of high-side power MOSFET.
VCC	9	Internal VCC LDO output. The driver and control circuits are powered by VCC. Decouple with 1μF ceramic capacitor placed as close to VCC as possible.
AGND	10	

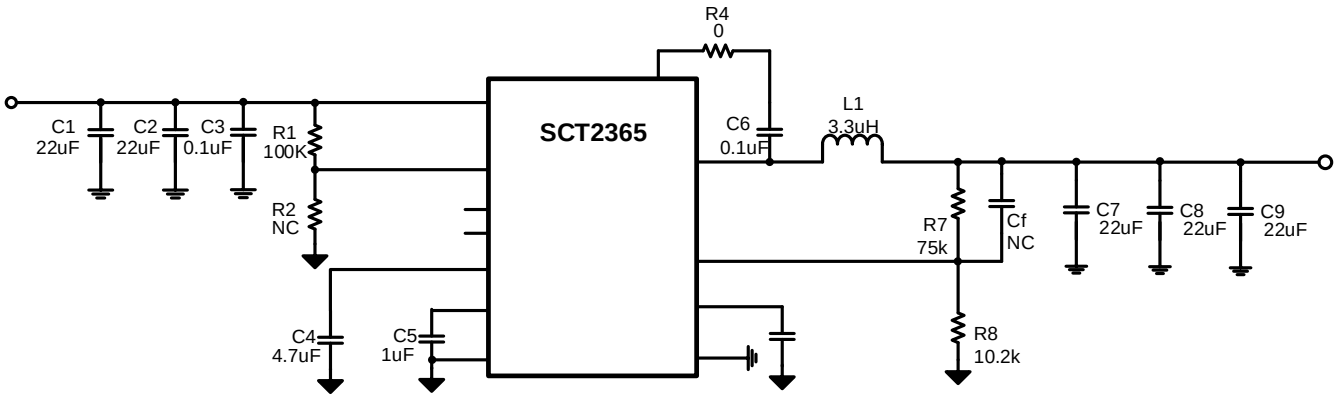



1
VIN
12
EN
9
VCC
6
MODE
5
SS
11
FB
10
AGND
4
EN_LDO
3
5.0V
VCC regulator
Bias and Reference
Mode Selection
On-time Generator
DC Error Correction
PWM Comparator
PG Comparators
Ramp Compensation
Control Logic and Protection
Bootstrap Regulator
Gate Driver
HS MOSFET
LS MOSFET
Current Sensing
OCP Comparator
HV_LDO
8
BST
7
SW
2
PGND

"

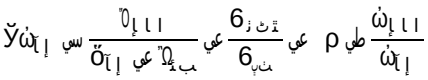
$$\ddot{O}_{\check{c}\check{c}} \text{ س } \grave{o}_{\check{c}\check{c}} \; ^{z} \frac{\sigma\acute{o}\ddot{o}}{\pi\wp\varphi\grave{\omega}}$$

-
-

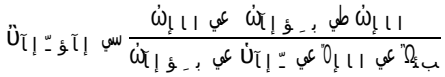


□ !

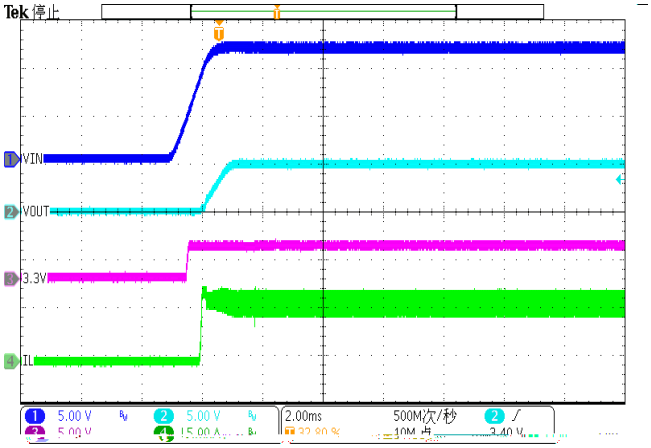
Design Parameters	Example Value
Input Voltage	12V
Output Voltage	5V
Output Current	6A
Output voltage ripple (peak to peak)	50mV
Switching Frequency	400kHz

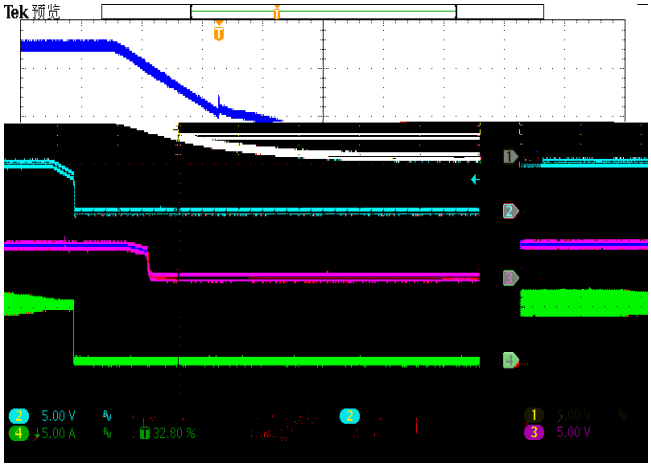


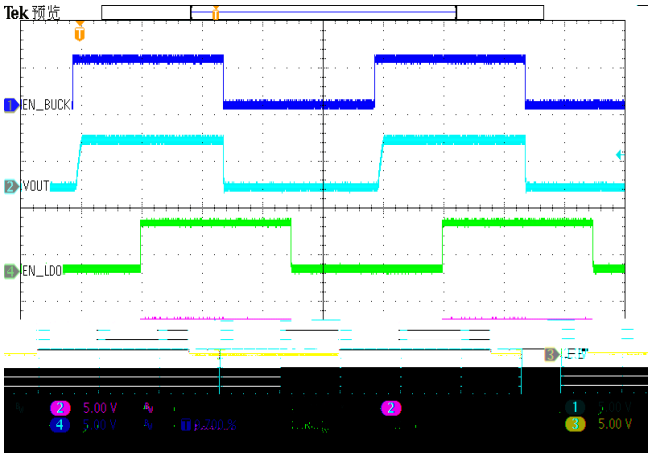
-
-
-

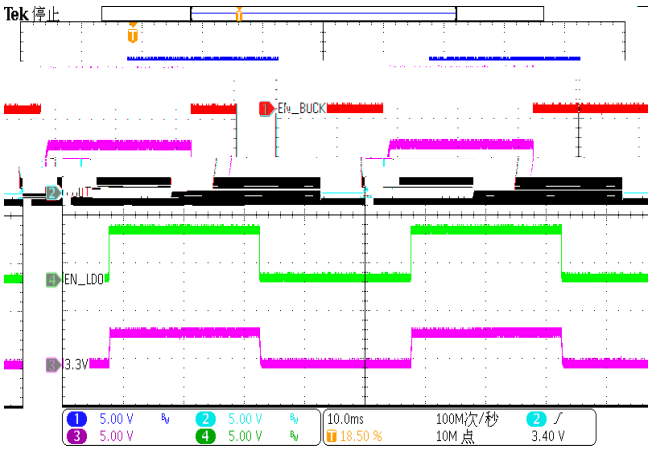


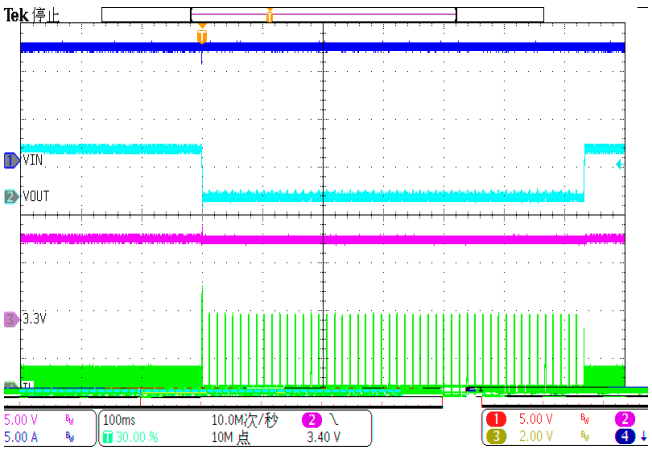
-

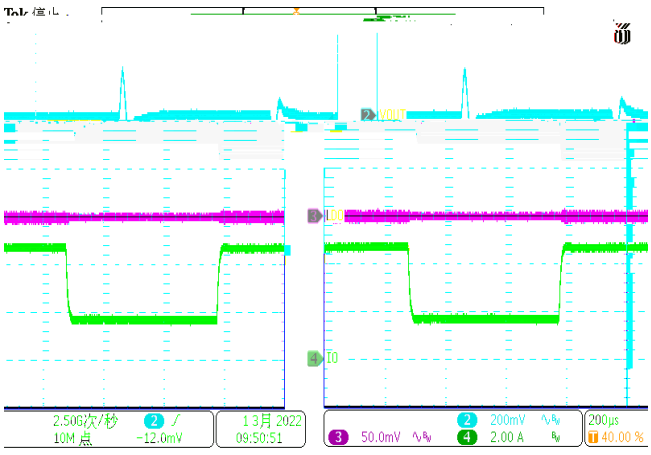

Tek 停止
VIN
VOUT
3.3V
IL
5.00 V
2.00ms
500M次/秒
10M 点

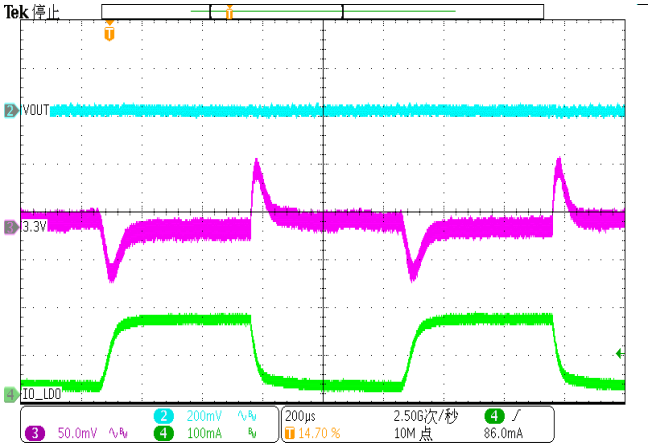

Tek 预览
5.00 V
5.00 A
32.80 %
5.00 V

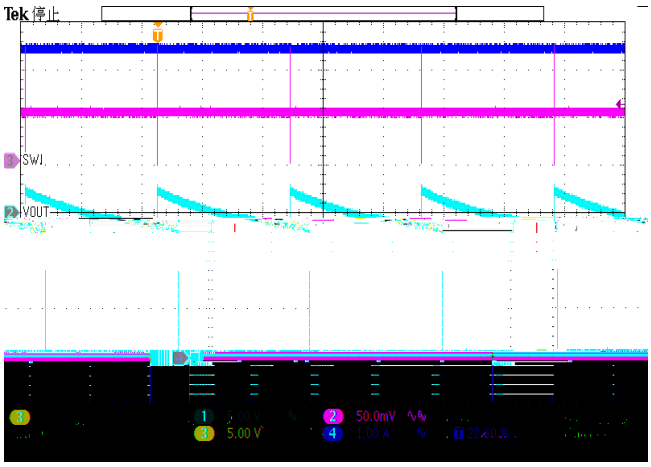

Tek 预览
EN_BUCK
VOUT
EN_LDO
5.00 V

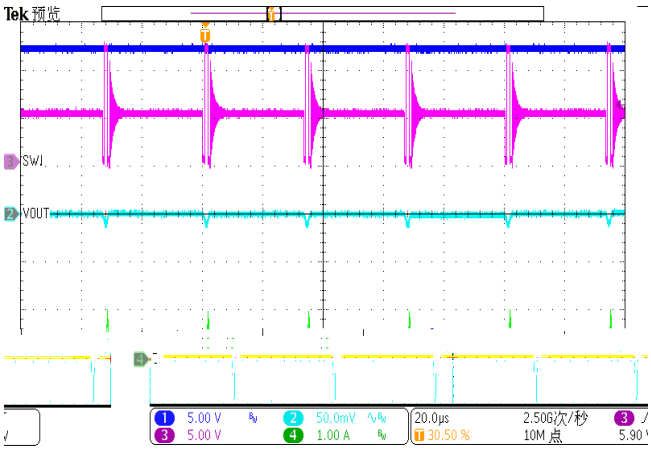

Tek 停止
EN_BUCK
VOUT
EN_LDO
3.3V
5.00 V
10.0ms
100M次/秒
10M 点
18.50 %
3.40 V

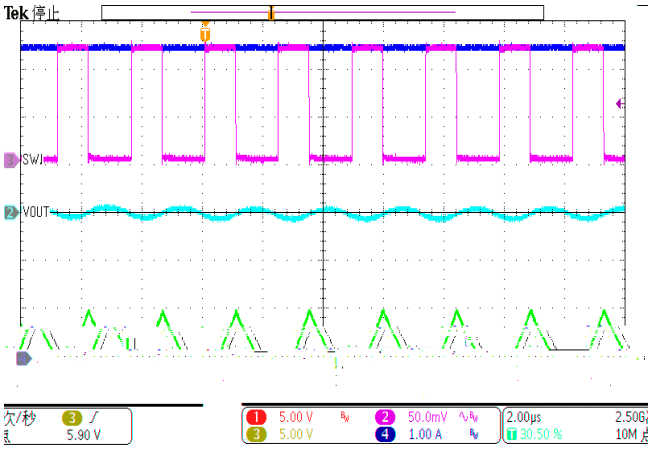

Tek 停止
VIN
VOUT
3.3V
5.00 V
5.00 A
100ms
10.0M次/秒
10M 点
30.00 %
3.40 V
2.00 V

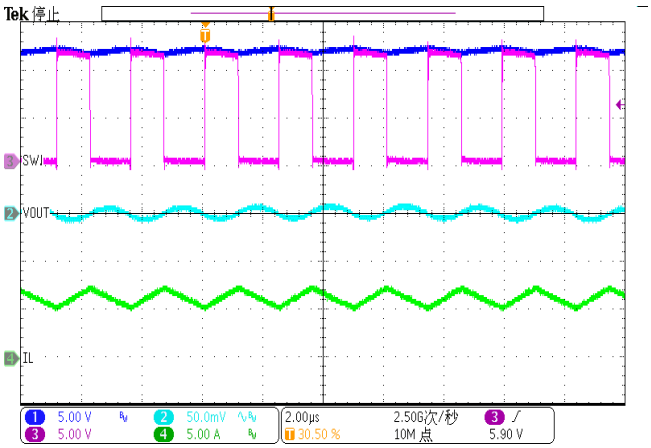

VOUT
IO
2.50G次/秒
10M 点
-12.0mV
13月 2022
09:50:51
50.0mV
200mV
2.00 A
200µs
40.00 %

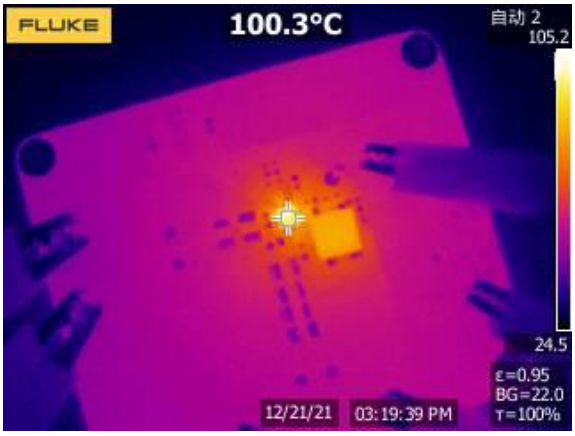

Tek 停止
VOUT
3.3V
IO_LDO
200mV
100mA
200µs
14.70 %
2.50G次/秒
10M 点
50.0mV
86.0mA


Tek 停止
SW1
VOUT
50.0mV
5.00 V


Tek 预览
SW1
VOUT
5.00 V
5.00 V
50.0mV
1.00 A
20.0µs
30.50 %
2.50G次/秒
10M 点


Tek 停止
SW1
VOUT
5.90 V
5.00 V
5.00 V
50.0mV
1.00 A
2.00µs
30.50 %


Tek 停止
SW1
VOUT
IL
5.00 V
5.00 V
50.0mV
5.00 A
2.00µs
30.50 %
2.50G次/秒
10M 点
5.90 V


FLUKE
100.3°C
自动 2
105.2
24.5
ε=0.95
BG=22.0
T=100%
12/21/21
03:19:39 PM

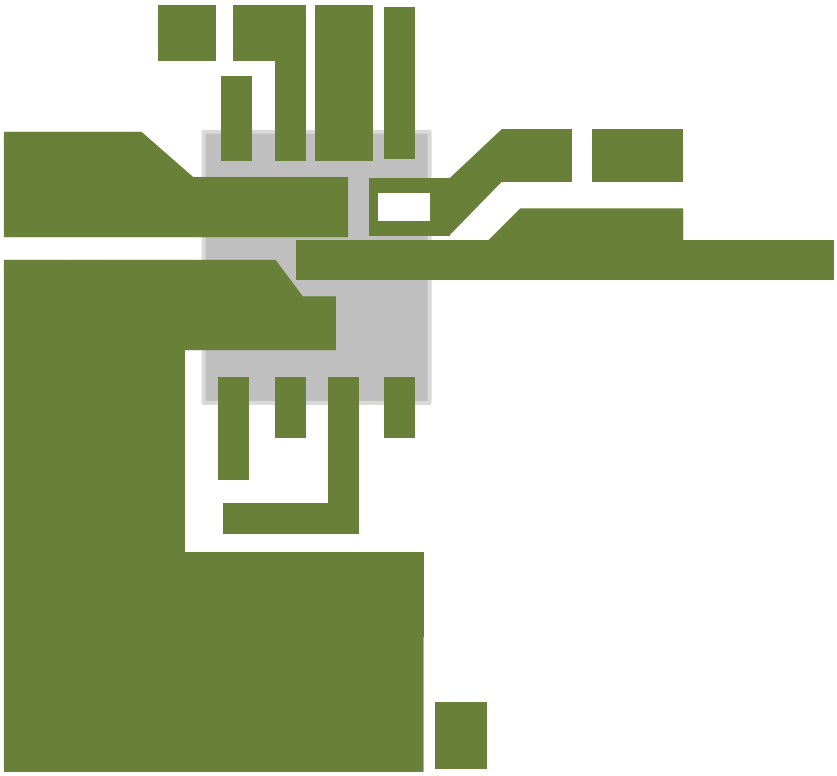
1.
2.

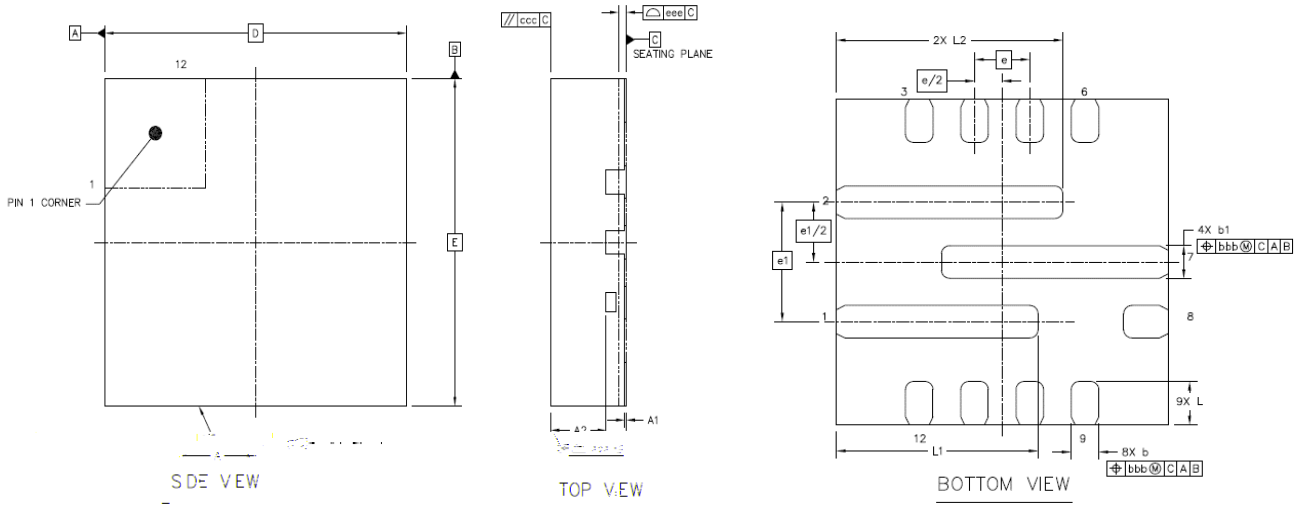
3.

4.

5.

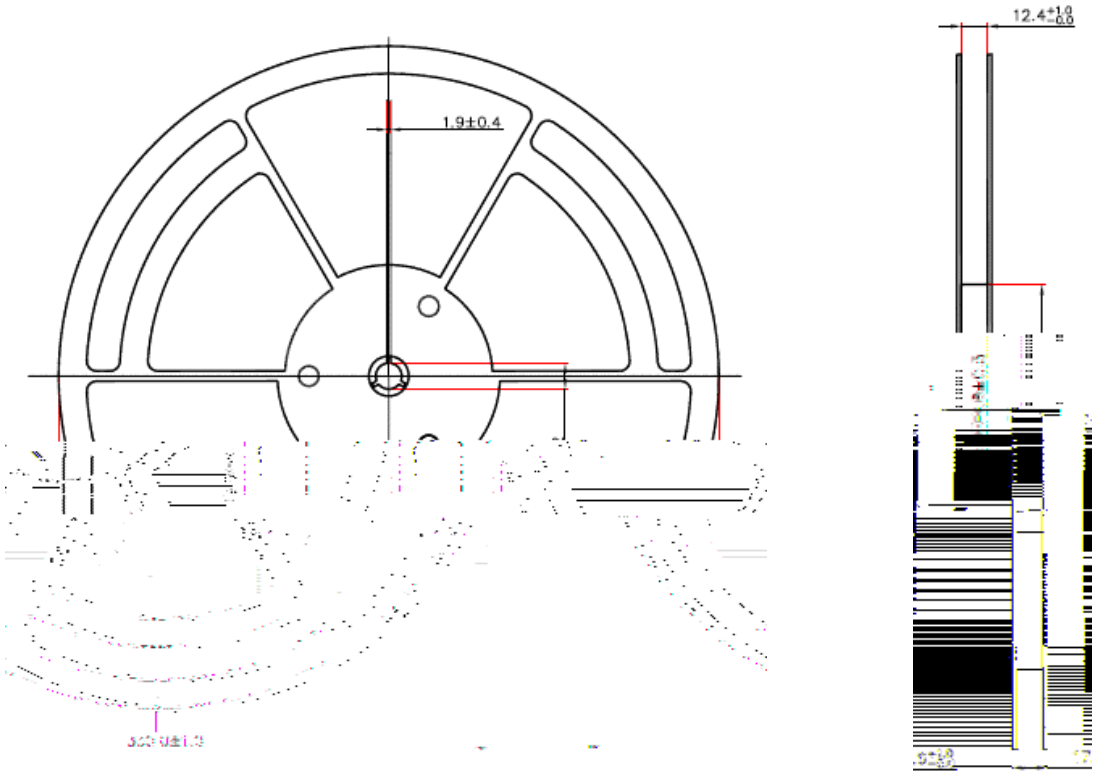
6.

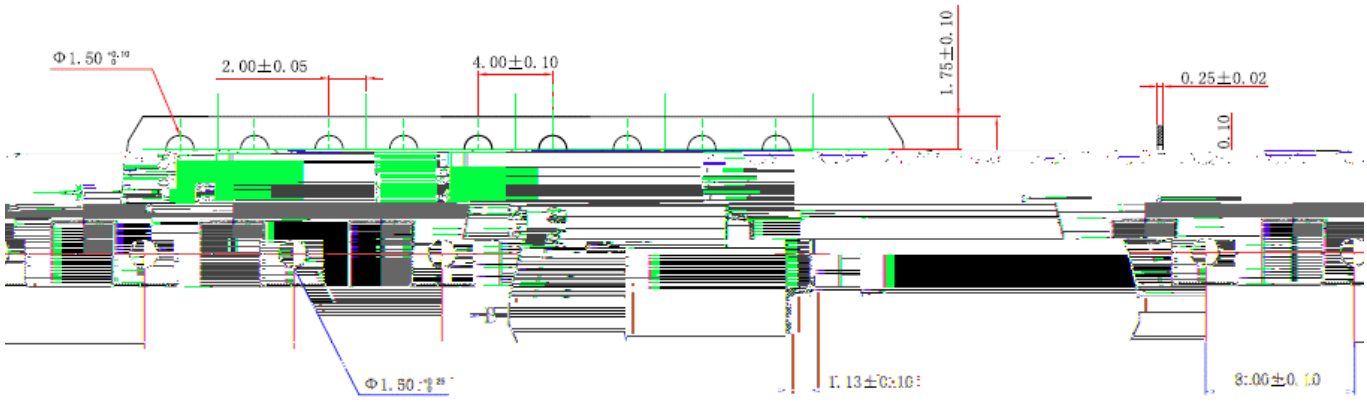



A
D
12
B
E
1
PIN 1 CORNER
SIDE VIEW
ccc C
eee C
C
SEATING PLANE
A2
A1
TOP VIEW
2X L2
e
e/2
3
6
2
e1/2
e1
1
4X b1
bbb M C A B
7
8
9X L
12
L1
9
8X b
BOTTOM VIEW

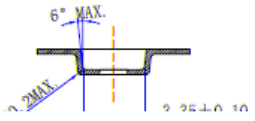
□			
□			

1.
2.
3.
4.
5.





SECTION B-B



SECTION A-A